SIGMA COMPUTER MEMO #26A

TO: E. Bloch

SUBJECT: Lookahead Section of the Sigma Computer

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This memo describes the Lookahead Section of the Sigma Computer. The material describes the equipment provided and functional operation of the system.

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LOOKAHEAD SYSTEM

I. Introduction

The purpose of this memo is to describe the operation of the Lookahead Section of the Sigma Computer. The material is organized in the following manner:

II Functional Location Within the Sigma Computer

The overall Sigma Computer is shown in Systems Drawing 00.00.00.0. To illustrate the functional location of the Lookahead, the data flow for a Floating Point Add-to-Memory operation will be traced through the system.

The Instruction Unit initiates the request for the instruction from the memory location specified by the instruction counter. The Memory Bus, in honoring the request, effects the transfer of the instruction from memory to the Instruction Unit Y register. The necessary index information is fetched within the Instruction Unit and the effective address generated. The specified operand is requested of the Memory Bus and the instruction operation code entered into one of the lookahead buffer registers. Acceptance of the memory request essentially frees the Instruction Unit for preparation of the next subsequent instruction.

The operand is returned by the Memory Bus to the lookahead where ECC information is interrogated for validity of the data. Assuming no in-valid conditions exist, the operation code and operand may be transferred to the Parallel Arithmetic Unit for execution. The execution consists of addition of the operand to the accumulator contents with the result returned to the lookahead for eventual storing to memory. This latter action essentially frees the Arithmetic Unit to begin execution of the next subsequent instruction, which has been undergoing preparation by the Instruction Unit and Lookahead.

The result to be stored is checked for validity and ECC generated within the look-ahead. The memory reference is initiated and acceptance by the Memory Bus for transfer to memory concludes the operation.

III Functions

Functionally, then, the look-ahead serves to provide those functions necessary to allow maximum utilization of execution equipment. The program interrupt feature of the Sigma Computer places additional sequencing functions upon the system. The primary functions performed by the system are:

A. Instruction Execution Sequencing

1. Receive indexed instructions
2. Receive and check operands
3. Transmit instructions and operands to the proper arithmetic unit
4. Receive operands to be stored
5. Initiate all store operations

B. Interrupt System Sequencing

6. Enter pre-set indicators into Indicator Register
7. Retain Instruction Counter value
8. Restore unused index modifications for interrupt

IV Register Definition

To perform these functions, four levels of buffer registers are provided, as shown in System Drawing 30.00.00.0. Each level is designed to completely buffer the information required by the Parallel Arithmetic Unit for execution of single operand, single operation type instructions. In general, instructions of the multi-operand (Cumulative Multiply) or multi-operation (Add-to-Memory) types require the use of more than a single level of buffering.

Each lookahead level requires the following registers to perform the instruction execution functions.

A. Operation Code Field (1 of 4) 36.00.00.0

This is an 11 bit field which specifies the operation to be performed at a particular level. The final bit is a check bit on the other ten. Instructions not entirely contained in a single level require this value only at the first level. In subsequent levels, this field will contain coded information for lookahead control purposes.

B. Operand Field (1 of 4) 31.00.00.0

This field contains 64 information bits and 12 check bits. It may buffer any of the following information:

1. The operand required for execution of the operation specified by the Operation Code Field.
2. Data to be stored in memory
3. VFL instruction execution information
4. Input-Output instruction execution information
5. Information for computer recovery

C. Lookahead Address Register (LAAR)

This 19 bit register, of which the final bit is a check bit, serves the entire lookahead to buffer an operand address when necessary for instruction execution. Instructions requiring the use of the LAAR are of the store type or those specifying as an operand the contents of an internal register.

Each level requires the following registers to perform interrupt system functions:

D. Indicator Field (1 of 4) 33.00.00.0

This 15 bit field represents the status of the indicators affected by indexing of the instruction contained at that level.

E. Instruction Counter Field (1 of 4) 32.00.00.0

The address of the instruction immediately following that instruction buffered at a level will be stored in the Instruction Counter Field of the same level. This value will be stored during an interrupt procedure for re-entry into the program following the correction routine. For multi-level instructions, the value as it appears in the final level only is valid for this purpose.

F. Instruction Counter Buffer (1) 32.00.00.0

This 21 bit field indicates the above defined instruction counter value which applies to the instruction being executed at a given time. It is transferred from the appropriate Instruction Counter Field as the instruction begins execution and is retained during interrogation of the program interrupt system.

For control purposes, each level contains he following information, which is used in conjunction with the operation code field.

G. Tag Bit Field (1 of 4) 36.00.00.0

This 8 bit field contains information concerning the status of information stored at the same level. The bits and their functions are described below.

1. Level Filled Bit (LF)

This bit applies to the Operand Field and indicates that the operand has been entered at the level.

2. Level Checked Bit (LC)

This bit indicates that the operand at the level has been checked and check bits converted to thos required by the particular operation.

3. Internal Operand Bit (INT)

This bit indicates that the operand required for instruction execution must be fetched from an internal computer register.

4. Instruction Counter Bit (IC)

This bit indicates that the value stored in the Instruction Counter Field of a particular level is valid for interrupt interrogation. It will indicate the final level associated with each instruction.

5. Lookahead Operation Code (LAOP)

This bit indicates that the value stored at the Operation Code Field of a particular level is for use by Lookahead control only.

6. Word Boundary Crossover Bit (WBC)

This bit in conjunction with $\overline{\text{LAOP}}$ indicates that the operand associated with the SAU instruction buffered at this level crosses a memory word boundary. In conjunction with LAOP, this bit indicates that the store data buffered at this level had ECC bits generated during the loading process.

7. No Operation Bit (NOOP)

This bit indicates that the instruction associated with this level is to be executed as No Operation.

8. Disconnect Bit (DISC)

This bit indicates the level should not participate in lookahead action. This is essentially a maintenance feature.

As will be shown, logical combinations of these bits will be coded to indicate further control information as the operations on the instruction progress through the Lookahead.

V. Sequencing Elements 38.00.00.0

The lookahead levels accommodate a maximum of four pre-accessed instructions and operands. To properly sequence the operation performed on each level, the system contains five counters which cycle through the levels, each counter performing a specific operation or series of operations.

1. Indexing Arithmetic Unit Counter (IAUC)
2. Operand Check Counter (OCC)
3. Transfer Bus Counter (TBC)
4. Arithmetic Bus Counter (ABC)
5. Store Check Counter (SCC)

The counter operations are essentially asynchronous in nature, i.e., they may be performing their particular function simultaneously on different levels providing full overlap throughout the system. The counter value indicates the level at which the function is being performed. The counters are interlocked such that no counter may pass another. This dictates proper sequencing of the operations performed on a level. The functions for which each counter is designed and the registers and data paths involved are discussed here in general terms as a basis for the control and timing considerations discussed in Sections VI-IX. The conditions necessary for initiating the action, the action itself, and conditions for advancing to the following level are discussed in that order for each counter.

A. Indexing Arithmetic Unit Counter

The function of the Indexing Arithmetic Unit Counter is to select the level next due to receive an instruction from the Instruction Unit.

In addition to the normal interlock preventing a counter from passing another, the IAUC is not allowed to re-enter a level until the SCC has left that level. This allows the enabling of an Instruction Unit load cycle immediately upon advancing the IAUC into a level. The type of loading enabled is dependent upon the status of the LAAR - i.e., - a store or internal fetch type instruction may not be loaded until the LAAR becomes not "busy". In addition, once the necessity of forwarding an operand within the lookahead has been recorded, Instruction Unit loading is suspended until the forwarding function has been accomplished.

Depending upon the type of instruction to be entered, the following fields and data paths may be involved. System Drawings 31.00.00.0 through 36.00.00.0 illustrate the fields in greater detail.

The Operation Code field will receive either the instruction operation code from the Instruction Unit Z Register or a lookahead operation code from the Instruction Unit-Look-Ahead Encoder.

The Operand field may receive information at the IAUC level via any of the following data paths, depending upon the particular instruction involved.

1. When the required operand is located in an external Memory location, the Memory request is initiated by the Instruction Unit with the IAUC value specified as the return address. The operand will be received at a later time via the Instruction Memory Out Bus (IMOB).

2. When the above Memory request is initiated, a comparison of the fetch address is made with the contents of the Lookahead Address Register. Satisfaction of this comparison indicates that the operand requested is already in the Lookahead for use by an "earlier" instruction. In this case, level identification information is set up and the Memory request cancelled. Thus, the operand may be "forwarded" at such time as it is available.

3. The operand may be received directly from the Instruction Unit via the Instruction Checker Out Bus (ICOB). This is generally the case when the specified operand is in Index Core Storage. This is also the case for store type instructions whose execution to the point of storing the result is effected entirely in the Instruction Unit.

4. VFL instructions require buffering in addition to the Operation Code Field in order to store all information required by the Serial Arithmetic Unit for proper instruction execution. The Progressive Indexing, Field Length, Byte Size, Offset & Bit Address values are entered into the Operand field via the ICOB in the first level associated with a VFL instruction. The operand or operands will then appear in subsequent levels.

5. The Control Word Address and Channel Address associated with Input-Output type instructions are buffered in the Operand field. These values are entered via the ICOB from the Instruction Unit during the loading process.

The Lookahead Address Register will receive the address to which information is to be stored, or the address of the internal register from which the operand must be fetched for execution of the particular instruction involved. If the instruction to be loaded is of the external fetch type and the LAAR is not "busy" i.e., no unexecuted store or internal fetch type instruction exists in the Lookahead, the register will receive the address of the operand involved. This will provide comparison information for the next subsequent instruction for forwarding purposes.

The Indicator Field receives the values of those indicators affected by indexing the instruction being loaded. These bits are generally transferred from an updated Indicator Register located in the Instruction Unit.

The Instruction Counter Field receives the proper instruction address from the Instruction Counter Adder located in the Instruction Unit.

The appropriate Tag bits will be set from the Instruction Unit Lookahead Encoder to properly identify the operations to be performed at the level.

An indication from the Instruction Unit that the loading process is complete allows the IAUC to advance to the next level as soon as the SCC interlock allows.

B. Operand Check Counter

The primary function of the OCC is to check the operand stored in the operand field and convert the check bits to those applicable to the Arithmetic Unit involved - i.e. - field parity for use by the Serial Arithmetic Unit and Residue check bits for use by the Parallel Arithmetic Unit. Both types of check bits are generated during each OCC check cycle and all are buffered in the check bit positions of the Operand Field. Only those operands from external memory require these functions since operands loaded directly by the Instruction Unit have the check and conversion performed during the loading process.

The check is initiated for the level selected by the OCC as soon after the Level Filled indication is received as the Lookahead-Instruction Checker In Bus (LAICIB) priority system will allow. Completion of the check cycle will result in the setting of the Level Checked bit and is an indication for the OCC to advance to the next level. This advance is, of course, contingent upon the interlock with the IAUC.

C. Transfer Bus Counter

The TBC controls the transfers of the instruction operation codes and operands to the working register of the proper Arithmetic Unit. This is generally true of instructions whose operands arrive from external memory or index core storage. For internal operands, this function is performed at the ABC level, since the action is contingent upon the status of a previous operation and upon the status of the interrupt mechanism.

The action of the TBC is contingent upon the status of the LF and LC bits indicating that the operand is ready for execution. The Parallel Arithmetic Unit receives the contents of the Operation Code field at the gates of the PAU Execution Register (via direct path) and the operand at the gates of the C register (via the Transfer Out Bus - TOB) together with an indication to begin pre-execution of the instruction.

In the case of a VFL instruction, the Serial Arithmetic Unit receives the contents of both the Operation Code field and the Operand field at the gates of the SAU Execution Register together with an indication to begin pre-execution.

In order to overlap the execution of one instruction with the check performed upon the results of the previous instruction, pre-execution is defined as execution of that portion of the instruction which does not require the modification of an addressable register. This latter action is contingent upon the status of the interrupt mechanism and is controlled by the ABC.

The TBC, after the transfer is performed, dwells with the information on the lines until such time as the proper Arithmetic Unit gates in and begins pre-execution. This signal allows the TBC to advance, contingent upon the OCC interlock, to the next level for pre-execution preparation.

D. Arithmetic Bus Counter

The primary function of the ABC is to control those functions necessary for proper operation of the interrupt mechanism. This includes entering the contents of the Indicator Field into the Indicator Register, updating the Instruction Counter Buffer, and, in the event of an interrupt, "marking" the remaining unexecuted instructions in the lookahead for proper handling by the SCC.

Secondary functions performed by the ABC include initiating the execution of instructions involving internal operands, selecting the level to receive store data from the Arithmetic Unit and effecting this transfer.

An indication that the previous instruction terminated with no program interrupt allows the modification of addressable registers to take place associated with the present instruction. After the Indicator Register and Instruction Counter Buffer have been set, if no internal register fetch or store operation is required, the ABC is free to advance, contingent upon the TBC interlock.

If the instruction involved is of the internal fetch type, the Operation Code and contents of the specified internal register are transferred to the Arithmetic Unit. The proper internal register is decoded from the contents of the LAAR and the transfer of the operand is performed via the Arithmetic Bus, where checking and check bit conversion is performed. An indication is given to the Execution Unit to begin execution and the response indicating acceptance allows the ABC to advance.

If, on the other hand, the instruction involved requires a store operation, the ABC dwells after entering interrupt information, until notified that the data is ready. The transfer is then performed to the lookahead register designated by the counter position for storage to external memory or Index Core Storage, as decoded from the contents of the LAAR. Storage to an internal register is performed directly from the Arithmetic Unit to the register involved. In all cases, the transfer takes place via the Arithmetic Bus. Completion of the store transfer allows the ABC to advance.

Termination of the previous instruction with a program interrupt indicates another form of action. No indicators or instruction counter values are transferred since doing so constitutes the modification of an addressable register. Instead, the level is interrogated to determine if interrupt recovery information is involved and those levels requiring this action are marked. The actual recovery function is performed by the SCC.

Recovery information buffering in the look-ahead stems primarily from the fact that the Instruction Unit updates the Index Core Storage information out of sequence. Prior to destroying the original contents of an index address, these contents are buffered in the look-ahead operand field. During interrupt procedure, restoring these values restores the computer memory to the proper status prior to entering the interrupt sub-routine. The index address involved for this operation is stored in the Operation Code field as a portion of a Lookahead Operation Code.

E. Store Check Counter

The primary functions of the SCC include controlling the check,

check bit conversion and storing of information to be written in memory. In addition, satisfying requests by the Instruction Unit for internal register contents, and interrupt restoration functions are performed by the counter.

Completion of the ABC function at a particular level is generally the indication for SCC to initiate the particular function required. Indication of completion is normally in the form of logical combinations of the tag bits and operation code field.

The lookahead initiates all storing operations for the Sigma computer. The memory area involved is decoded from the contents of the LAAR. The operation involved may be received from the Instruction Unit directly in the case of indexing store type instruction or from the appropriate Arithmetic Unit in the case of arithmetic store type instructions.

The latter type store to external memory requires the initiation of a priority request to the LAICIB system, where parity check and ECC generation takes place. Completion of the check and conversion function allows the store request to be made to the Memory Bus Unit. The operand transfer is effected via the Lookahead Memory In Bus (LAMIB). The address is decoded by the Memory Bus Unit directly from the contents of the LAAR. Acceptance of the information allows the SCC to advance.

Should the LAAR contents indicate Index Core Storage, parity check and check bit conversion are performed during the transfer of the data via the LAICIB to the Instruction Unit X Register. The A_d dress is gated from the LAAR to the Index Core Storage Address Bus and an indica tion given to perform the Clear-Write cycle. Completion of this cycle allows the SCC to advance.

Those instructions for which the store operand is received directly from the Instruction Unit require no check and conversion cycles since these functions are performed during the loading process.

Since the Instruction Unit has no direct access to the contents of addressable internal registers, requests for their contents must be buffered in the Lookahead. At the proper time, the information is fetched by the Lookahead and transferred to the Instruction Unit. The transfer from the internal register is performed at the ABC level with the data returned to the level involved. The SCC then transfers the information via the LAICIB to the appropriate Instruction Unit working register. Completion of the transfer allows the SCC to advance.

After a Program interrupt has been detected, the SCC restores the index values to Index Core Storage. As in the case of an index store instruction, the operand is transferred via the LAICIB to the X register. The address, however, is gated from the Operation Code field to the Index Address Bus and the Clear-Write cycle initiated.

F. Forwarding Mechanism

The ability of the Lookahead to forward information already available within the system is essentially independent of any particular counter. This is required to take full advantage of the mechanism. Controlling the function is achieved by a set of control triggers indicating the particular level to which the contents of the LAAR applies. One of four triggers remembers the IAUC value at the time the LAAR is loaded and specifies the level from which the data is to be forwarded. The IAUC position at the time a comparison is detected specifies the level to which the data is to be forwarded. This information defines the origin and destination of the data.

The time at which the forwarding may take place depends upon the status of the information requested. If the operand to be forwarded is associated with a store instruction, the forwarding may take place after the Memory Bus has accepted the store request. If the operand is associated with fetch type instruction, the forwarding may be effected immediately after the word has returned from Memory and has been checked.

The actual transfer takes place via the LAICIB. Completion of the transfer results in setting the LF and LC bits in the "to" level. The forward control bits are updated for further forwarding function- i.e. - the "from" indication is altered to indicate the new level to which the contents of the LAAR apply.

VI. Instruction Preparation Control Definition

The Level Filled and Level Checked tag bits essentially separate the instruction preparation and instruction execution phases of lookahead action. "Level Filled" means the operand required for transfer to the execution unit has been received by the lookahead from either external memory or the Instruction Unit or that no operand is required at this level. "Level Checked" means that this operand if any has the proper check bits as it appears in the lookahead.

These two bits do not apply to an internal register when specified as an operand nor do they apply when a lookahead level is "filled" and "checked" due to receiving information to be stored from the SAU or PAU.

A. Lookahead Loading

The IAUC advance into a level resets the LC and No Op tag bits at the new level to disallow false interrogation by another counter of "old" information. The advance also sets an "IAUC Advance Enables Sequence" trigger which participates in a signal to the Instruction Unit enabling that unit to enter an instruction. Other considerations given the enable signal include the fact that (1) lookahead is not in the process of restoring unexecuted information (housecleaning mode) and (2) that the level in question is not disconnected, as evidenced by the Disconnect tag bit.

During housecleaning mode, no load enable signal is given until housecleaning is complete. A level which is disconnected allows the IAUC to advance again and attempt to enable the loading of the next level.

(This "advancing over" a disconnected level is normal operation for all counters.)

1. Enabling the Load

The type of instruction loaded is dependent upon the status of the LAAR. A type I + II Enable signal allows the entering of any level of buffering which does not require the use of the LAAR. Its presence indicates only that the level is available for loading.

A type III Enable signal allows entering any level of buffering which requires the use of the LAAR. Its presence indicates that the level is available for loading and that the LAAR is available as evidenced by the absence of an LAAR Busy signal.

2. The Loading Process[1]

The response to the Load Enable signals are the actual Load Pulses from the Instruction Unit. These Load Pulses are of three types. Load Pulse Type I indicates that the level being loaded 1) does not entail an external memory operand fetch and 2) does not

1 Appendix IV-p. OA

require the use of the LAAR. Load Pulse Type II entails an external memory fetch and Load Pulse Type III requires the use of the LAAR.

The loading process is normally accomplished in two basic clock cycles. The first half of any type Load Pulse (Load Pulse 1/2) resets the "IAUC Advance Enables Sequence" trigger thus disallowing any further Load Enable signals until the IAUC advances.

The second half of each type Load Pulse is used to properly identify the level status.

A Load Pulse Type I, by definition, indicates that either (1) the operand is loaded directly by the Instruction Unit or (2) no operand is required at this level. In either case, no operand preparation is required; thus, LF and LC are set directly. The signal also resets the FROM bit in the level and sets a "Load Pulse Memory" trigger which allows the IAUC to advance to the next level when the interlock conditions are such that (IAUC $\neq$ SCC - 1). Anticipation equipment is provided to allow the IAUC to Advance and to allow a new Load Enable Type I + II signal and Load Enable Type III signal (the latter contingent upon no LAAR Busy signal) to the Instruction Unit during the Load Pulse Type I 2/2. This allows successive level loading as fast as is practical. In either event, the Load Pulse Memory is reset with the first sample following the advance of the IAUC.

A Load Pulse Type II indicates that the operand required for execution is being requested by the Instruction Unit of the BCU. This type pulse may persist longer than two basic clock pulses and completion of the loading process must be contingent upon one of two signals from the BCU.

Equipment is provided to compare any fetch address used by the Instruction Unit with contents of the LAAR. This is necessary to prevent fetching false information out of turn. The comparator is enabled for this purpose whenever the LAAR is Busy.

When the Instruction Unit requests the services of the BCU for operands returnable to the Instruction Unit, an address compare signal merely blocks the fetch request until such time as the LAAR becomes not busy. This indicates that the store has been executed and the BCU proceeds to honor the request.

Since the Lookahead provides the ability to "forward" operands from level to level to elimate unnecessary memory references, the comparison equipment is enabled by Type II Load Pulse. This signal defines requests for operands returnable to the Lookahead level designated by the IAUC value. An address comparison here results in 1) blocking the fetch request and 2) setting a "Forward Cycle Required" trigger in the Lookahead. The comparison signal, delayed

one clock cycle, is sent to the Instruction Unit to terminate the Type II Load Pulse signal. In this case, Load Pulse Memory is not set and the IAUC does not advance until the forwarding function is complete.

The action upon no comparison is contingent upon BCU acceptance of the request. The coincidence of Load Pulse Type II and Memory Fetch Accept sets Load Pulse Memory, enabling the IAUC to advance. In addition, if the LAAR is not busy, the address is gated into the LAAR, the IAUC value remembered in the form of "From" bit identifying the level to which the LAAR applies and the Store Executed trigger is reset.

Anticipation equipment identical to that provided during Load Pulse Type I again allows new Load Enable signals during a Load Pulse Type II.

The Load Pulse Type III identifies the level being loaded as an internal operand fetch level or a store level-i.e. the LAAR is required for proper execution. The sample selected by the Load Pulse Type III 2/2-1) gates the address to the LAAR, 2) sets the LAAR Busy trigger, the appropriate From bit identifying the level, Load Pulse Memory, the LF and LC tag bits, and 3) resets the Store Executed trigger.

Type I + II Enable signals only are anticipated during a Load Pulse Type III.

Many other signals are exchanged between the Instruction Unit and the Lookahead during the loading process to gate in the proper information fields and condition the proper tag bits and indicators from various error and alarm lines. These signals are received from any of three Instruction Unit areas due to packaging and timing consideration. These signals are shown in chart form in Appendix II, together with their gating and conditioning functions.

The loading sequence for each type load cycle is shown in timing bar chart form in Appendix IV.

Special Considerations:

Certain control lines shown in Appendix II require special mention. Many are self-explanatory and only define gating and conditioning the buffer registers.

1. A limited number of Type III Load Pulse sequences are such that the data transfer involves an ECC check and possible correct cycle over the LA-I Bus checker. Thus, termination of the Load Pulse signal must be contingent upon the single ECC error signal. This type transfer is identified by the control line ECC CHECK LOAD. The possible correct cycle following is identified by ECC CORRECT LOAD. The logic involved in determining when the load may be properly terminated is shown in Appendix II.

2. A variation in the defined handling of a Type II Load Pulse exists when it is for the purpose of loading the first level of the PAU Multiply and Add(*+) instruction. In this case, the control line MPYC LOAD E. Mto LA is used, if the address does not compare with the contents of the LAAR, to inhibit 1) gating into the LAAR, 2) setting the From bit and 3) resetting the STORE EXECUTED trigger. The purpose of this action is to allow forwarding of the Factor register contents when the PAU Load Factor (LFT) instruction is followed immediately by Multiply and Add. Since the two levels involving the Factor register contents are separated by the first level of Multiply and Add, (See Appendix III) the above action prevents changing the LAAR contents, thus, preserving the possibility of address comparison.

3. Under special conditions the Instruction Unit in attempting a Type II Load sequence, discovered this action to be invalid and terminates the load.

However, the IAUC Advance Enable Sequence has been reset and thus, the Load Enable signals have disappeared. The signal Type II CANCEL MEMORY replaces this trigger participation in the Enable signals to allow the level to be "reloaded".

B. Operand Preparation[2]

The check and check bit conversion of external memory operands are performed at the Operand Check Counter level. The OCC Advance Enables Sequence trigger, set by any advance of the counter, performs essentially the same function for the OCC as its namesake does for the IAUC - i.e., it allows the counter function to be performed only once at any one level. This philosophy is true for all counters.

By definition, the OCC function is required only of those levels loaded by a Type II load Pulse with no address compare.

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1. Operand Check

The BCU precedes, by one clock cycle, the returning memory word with one of four Memory Select pulses selecting the level to receive the operand. The LF Indication at each level is in the form of two triggers--an Execute (LF-E) and its associated Memory (LF-M) trigger.

LF-E is set by the free sample selected by the Memory Select Pulse. LF-M is set by the free sample selected by LF-E $\overline{M}$ which also gates in the operand and ECC bits to the appropriate level. Should an error in the form of a Memory Check indication from the BCU occur, the NO Op tag bit and the Instruction Reject (IJ) indicator in the level are set.

The coincidence of (LF-E + LF-M) $\overline{\text{LC.}}$ $\overline{\text{DISC.}}$ OCC ADV EN SEQ forms a request signal to the LAICIB priority system. Operand checking has 3rd priority on the I Checker Bus and is delayed by any check or correct cycle in process (O Priority), lookahead store check request (1st priority) or lookahead forward request (2nd Priority). It, in turn, delays any lookahead to Instruction Unit request (4th Priority). The sample selected by the response honoring the request sets Operand Check E trigger which participates in timing the data transfer. (see OCC Timing Diagram - Appendix IV)

This trigger gates out the operand from the level selected by the OCC to the LAICIB while the first half (E. $\overline{\text{M}}$) is sent to the I checker as an indication to check ECC. Operand Check E. M selects the sample which gates the data, field parity and residue check bits back into the same level. LC is also set if the check results in no single ECC error. The OCC advance takes place in this case on the same sample if the interlock allows; other wise, on the first sample after the interlock disappears.

2. Operand Correct

The action upon detection of an ECC error results in setting Operand Correct E. The total operand gate out signal is, then, the "OR" of these triggers.

The Correct timer provides an additional two clock cycles and terminates by setting the LC bit and, if the error proves uncorrectable, by setting the No Op tag and IJ indicator at the level. The data and check bits are again gated into the operand field with Operand

Correct E. M. (The original ECC bits have been latched at the I Checker-in-bus throughout the correct operation.) The OCC advance takes place in this case on the sample selected by E. M. of the Correct timer if the interlock allows; otherwise, on the first sample after the interlock disappears.

This latter advance condition, (LC . $\overline{\text{INTERLOCK}}_{O-I}$) also provides the advance over those levels loaded by a Type I or Type III Load Pulse where LF and LC are set directly.

3. Special Considerations

An exception to the above action occurs when the Maintenance Console panel keys are addressed as an operand in the maintenance mode of operation. The fetch, controlled by the BCU, returns data with no associated ECC bits to the lookahead.

To identify this type of operation, the Instruction Unit codes the preparation tag bits (INT . $\overline{\text{LF}}$. $\overline{\text{LC}}$). The Memory Select results in (INT . LF. $\overline{\text{LC}}$). The signal to the I Checker to Check ECC is suppressed and an identically timed signal to merely Generate Parity and Residue is given. Finally, the Operand Check E. M forms the normal coding of such a level ($\overline{\text{INT}}$. LF . LC) by resetting the Internal tag as well as setting LC. For consistency, this bit is always reset by Operand Check E. M.

C. Forwarding Action

The request for forwarding an operand from one level to another within the Lookahead is set up at the time the Instruction Unit attempts to fetch an operand for the lookahead and discovers an address comparison between the required operand and the contents of the LAAR. These conditions are remembered in the Forward Cycle Required trigger.

The operand to be forwarded may be the results to be stored following a store type instruction or it may be an operand used in a previous non-store type instruction. A variation in handling these two types of forward operations comes about due to differing check bit formats. The former operand, when ready for forwarding exists in the lookahead with ECC bits and, therefore, requires check bit conversion, while the non-store operand exists with the required lookahead field parity and residue already available.

To identify these conditions, a status triggers is set up at the SCC level. When the LAAR becomes not busy following a store operation, the Store Executed trigger is set. The trigger remains set until either a forward cycle takes place or the contents of the LAAR change.

1. Forward Check

The actual forward function is initiated when the LAAR becomes not busy. This insures that the data is available as well as that the Store Executed trigger is in that state which properly identifies the checking conditions. For the store type forward, the coincidence of (FWD CYC REQ'D . NO LAAR BUSY . STORE EXECUTED) is sufficient to form a request (2nd Priority) to the LAICIB priority system.

For the fetch type forward, the Level Checked tag bit is necessary in the origin level to indicate that the data is available. For packaging purposes the data from a single register may only be gated to one destination at a time. (This is due to the single unit of current available from the gate out distributor on the 2RG card used throughout the operand fields.) Thus, an additional restriction for the priority request is required to insure that the TBC is not at the origin level.

This prevents the possibility of this counter action gating the requested operand to the execution unit at the time the priority request is honored and the same operand gated to the LAICIB for forwarding. The total request is thus, (NO LAAR BUSY . NO STORED EXECUTED . FWD CYC . REQUIRED . LCi . FWD FROMi . NO TBCi) where i = level 1, 2, 3, or 4.

The sample selected by the line honoring of the bus request sets the Forward Check E timer. This trigger gates out the data and check bits from the level selected by the From bit. The first half of the timer E . $\overline{M}$ resets Forward Cycle Required trigger and, with either Store Executed or its absence, requests the checker to either Check ECC or Check LA Parity, respectively. Forward Check E . M gates in the data, field parity and residue to the level selected by the IAUC. In addition, if the check results in no single ECC error, 1) the Store Executed trigger is reset, 2) LF and LC tag bits are set in the destination level, 3) all From bits whose value do not agree with the IAUC value are reset, (this effectively changes the From bit to specify the new level to which the LAAR applies), and 4) Load Pulse Memory is set to allow the IAUC to advance.

2. Forward Correct

The action upon detection of a single ECC error is essentially the same as that for operand check and correct. The data is gated out for an additional two clock cycles and the above functions are performed by the sample selected by Forward Correct E. M (See Appendix IV).

In addition, if the error proves uncorrectable, the No Op tag bit and IJ indicator are set in the destination level.

3. Special Considerations: Absolute Forwarding:

It is possible for forwarding to specify the origin and destination of the data as the same lookahead level.

For this case, the logic described thus far for requesting bus priority for a non-store type operand fails since the LC tag is reset by the IAUC advance into a "new" level. This special case is remembered in the form of the Absolute Forward Required trigger. Thus, the final logic forming the priority request becomes (NO LAAR BUSY . ABSOLUTE FORWARD REQUIRED). The normal bus transfer is made in this case.

Forward No Op Conversion:

An additional complication arises from the fact that the data requested may be in error or even non-existent due to the instruction associated with the origin level being rejected. This case is detected by agreement of the From bit and No Op tag. Since a store instruction which is rejected does not result in the setting of Store Executed, it is not possible to request that a check be made on ECC bits, thus no correct cycle is possible.

For simplicity, the normal fetch forward function results with perhaps non-meaningful data being transferred and Forward Check E. M. results in the setting of the No Op tag and IJ indicator in the destination level. In addition, all From bits are reset. This condition disables the address comparison equipment, thus preventing any further forwarding action until the contents of the LAAR change.

Finally, to prevent the possibility of the above two special cases arising together, the detection of No Op i. FROM i when the IAUC advances from level (i - 1) to i results in resetting From i. This again disables the compare mechanism to prevent setting up forwarding under these conditions.

VII Instruction Execution Control Definition:

The preparation functions performed by the IAUC, OCC and FWD mechanisms are reasonably uniform and are controlled by tag bit combinations. The variations encountered in the execution functions performed by the TBC, ABC and SCC, however, are too numerous to warrant individual tag bit identification. Since the operation code field is used to buffer "real" instruction operation codes for the execution units in the first level of PAU and SAU instructions only, these triggers are available at the remaining levels for specifying lookahead operations. That is, this field contains a "Lookahead Operation Code" when so designated by the presence of the LAOP tag bit at the level.

Each instruction is defined regarding the number of lookahead levels required and their identification code in Appendix III. In general, a separate lookahead level is reserved to buffer information for each fetch and for each store function required by the instruction. Additional buffering restrictions may require additional lookahead levels. For example, the operand field of the first level associated with an SAU instruction is used to buffer additional operation code information; thus, an entire level (op. code level) is used to transfer this information to the SAU. The operand (or operands) required will appear in the next "fetch" level (or levels). Subsequently, any store data will be transferred from the SAU to the following level (or levels). Finally, when progressive indexing is specified, a level is reserved to buffer the "pseudo store" involved due to the Instruction Unit modifying Index Core Storage out of sequence. Thus, Appendix III shows a total of six lookahead levels required to process an SAU Add-to-Memory with progressive indexing. This is an extreme case and shows the need for each level to be processed by the execution counters and made available for re-loading during the execution of a single instruction.

Appendix III also shows, for each level, the array of bits in the Lookahead Operation Code and Tag Bit fields used to identify the functions to be performed. For convenience, this array is represented in octal notation consistent with the Definition of Level Designation. It should be noted that this represents the status of the Operation Code and Tag Bit fields upon termination of the Instruction Unit loading process. Thus, the LF and LC tag bits will change as any necessary preparation function are accomplished.

The execution counter functions for each level are shown in timing chart form in Appendix IV. These charts define the action taken by the TBC, ABC and SCC when the level is to be 1) executed normally 2) rejected due to the No Op tag bit, or 3) interrogated for housecleaning action. Due to the overlap of instruction preparation, it should be clear that any level may exist in the lookahead to be handled in any of these three major modes of operation.

The TBC functions begin only when $LF_i \cdot LC_i$ indicate that the information is valid and are timed by the Transfer Bus Timer (T-timer) triggers, E and M. These functions include the transfer of PAU and SAU operation codes and operands (not internal) to the execution units during normal operation, and initiating the pre-execution phases of these instructions.

The ABC functions are not only contingent upon the fact that preparation functions are complete, but that the Interrupt Mechanism has been reliably interrogated. The course of normal ABC action entails those functions necessary for execution which require the modification of an addressable register. On the other hand, if a program interrupt occurs, overlap is suspended in preparation for handling the remaining "unexecuted" levels of lookahead in a special manner (Housecleaning Mode) for any necessary restoration functions.

The equipment used to determine the state of the Interrupt Mechanism consists of an indication that all units have set into the Indicator Register a record of any abnormal conditions arising during execution of a particular instruction. Since such indicator settings may arise from any of a number of non-synchronous units, each units participation must be recorded and only when all units have "reported", can the interrupt line be reliably interrogated.

For this purpose, the lookahead contains a bank of "test" triggers. In each case, the sample selected to set the trigger is timed identically with the sample selected to gate the information into the Indicator Register.

Execution Unit Indicator Test

This trigger records the fact that the execution unit involved has entered all indicators associated with execution of instruction n.

Lookahead Normal Indicator Test

This trigger records the fact that the lookahead has entered all indicators associated with executing instruction n.

A-Checker Indicator Test

This trigger records the fact that the possible error detected during the normal arithmetic result check of instruction n has been entered.

Store Check Indicator Test

This trigger records the fact that the possible error detected during the SCC check and check bit conversion cycle for store instruction n has been entered into the Indicator Register. This trigger, unlike the others, is normally on and is reset as an ABC function only when it is evident such a check cycle will follow.

It should be noted that each trigger must be set following each arithmetic unit instruction regardless of whether any abnormal condition actually occurs.

The sample selected by coincidence of all triggers is used to memorize the state of the interrupt mechanism. (For speed purposes, when all other units have reported, and no A-checker error occurs, the A-Checker Indicator

Test trigger is not set and the interrupt mechanism memorized immediately.) The MAR MODE trigger remembers the normal condition, while the Interrupt Next Instruction trigger records the interrupt condition. This same sample resets the test triggers thus releasing them to record the indicator settings for instruction n + 1.

Since the interrupt mechanism must be interrogated following any instruction, an alternate method is used to determine the final indicator setting for non-arithmetic instructions (or No Oped arithmetic instructions) since the execution units are not involved. The Lookahead No-Op Indicator Test trigger records the last lookahead indicator setting for these instructions and since the lookahead is the only unit involved, the interrupt line is memorized on the basis of this and the Store Check Indicator Test triggers only.

It should be clear that the memorization due to coincidence of the test trigger settings for instruction n define the action to be taken on instruction (n + 1). For speed purposes, the PAU duplicates this equipment and, in certain cases, it is the responsibility of the lookahead to properly sequence this PAU mechanism as well as the local equipment.

The primary ABC action at any level is to effect the transfer of the Indicator Field to the Indicator Register and the Instruction Counter field to the Instruction Counter Buffer. These functions are timed with the Indicator Transfer Timer. Subsequently, if necessary, an internal operand (denoted by INT tag bit) is effected and timed with the Arithmetic Bus Timer (A-Timer). On the other hand, if store data is to be transferred from the execution unit, this transfer is also timed by the A-Timer.

The memory area involved for store data transfers is decoded directly from the contents of the LAAR. For index or external stores, the transfer occurs from the execution unit to the lookahead. The indication for the SCC to complete the store operation is the ABC reset of the LF tag bit. Thus, for all SCC action, the tag bit combination $\overline{LF} \cdot LC$ must occur. In this manner, the ABC selects those levels for SCC action, essentially filtering out the Instruction Reject and Lookahead Housecleaning complications for the SCC decoder.

The presence of TBC, ABC and SCC at a level establishes a d.c. gate out of the Operation Code and Tag Bit field of that level to the respective decoders. In general, a single decoder exists for each counter. (An exception exists for the TBC decoder identifying 1st levels of PAU instructions where, for speed purposes, a separate decoder exists at each level, thus preserving level identification.)

A. PAU Instruction Sequencing

The PAU instruction set has been classified for lookahead purposes into four categories: (See Appendix III, F.P. Loading Sequences)

1. Non Store Operations (single level)
2. Store Operations (single level)
3. Fetch and Store Operations (two level)
4. Multi-fetch Operations (two level)

Each category must be considered for variation of the fetch levels

specifying a) non-internal and b) internal operands.

1(a) Non Store Operations (non internal operands-Appendix IV p. 31

The action of the TBC is identical for the first level of all (not internal) PAU instructions. These levels are identified by the coincidence of $\overline{LAOP_i} \cdot \overline{INT_i} \cdot OP8_i \cdot \overline{OP9_i} : LF_i \cdot LC_i$. Normal action by the counter is identified by the absence of ($NOOP_i$) and (NOOP MODE) status trigger (designating Instruction Reject action) and by the absence of Lookahead Houseclean Mode trigger.

The Operand and Operation Code fields are gated to the PAU with the d.c. decode line. The information will appear at the input gates to the C register and PAU Execution Register two clock cycles later. Thus, T-timer E is set by the first sample selected by the decode line. Coincident with T timer $E \cdot \overline{M}$, two signals are given, one indicating that the PAU may Gate In Op Code and Start and the other to Gate In TOB to C. The PAU, if not ready to accept the information immediately, must remember these signals. No further TBC action occurs until the pulse PAU 1st Cycle (To) is received indicating that the information has been accepted. This pulse sets the 1st Cycle Memory trigger indicating the TBC may advance. The advance takes place on the sample selected by PAU 1st Cycle if no interlock with the OCC exists, or on the first sample selected by 1st Cycle Memory following the disappearance of this interlock. First Cycle Memory is reset by the first sample following the advance.

To again prevent the possibility of gating the operand to two locations simultaneously, if forwarding is in process from the level at which the TBC attempts to gate to the PAU, the TOB gate out and setting of T-timer E are delayed until the forwarding function is complete.

The only ABC function required for the non-store type is the transfer of Indicators and Instruction Counter Fields. These fields are gated out to their respective destinations by the d.c. output of the ABC position itself. Selection is then made as to what input gates to activate. These gate in signals are samples selected by the Indicator Transfer Timer; thus, the set condition for Indicator Transfer E is met only when preparation functions are complete ($LF \cdot LC$) and the previous instruction caused no program interrupt (MAR MODE).

The Indicator field of each lookahead level has been classified into three main categories. This is due to the variations of handling these categories during the three major modes of lookahead operation. The definition of transfer for each category:

[1]

Instruction Exception ($\overline{XR}$) Indicators

These are gated into the Main Indicator Register from each level

1. IR-OP-AD-DS-DF-IF

during Normal Operation and Instruction Reject Action.

Index Result (XR) Indicators[2]

These are gated into the Main Indicator Register from distinctly coded Instruction Unit instruction levels during Normal Operation only.

Conditional Machine Check (CNIDC) Indicator

This single indicator is gated into the Main Indicator Register from each level during Instruction Reject Action and Housecleaning Action.

The gate in signal is timed with Indicator Transfer Timer E·M. The gate into the Instruction Counter Buffer is activated only on levels tagged with the IC bit and is timed with $E \cdot \overline{M}$ of the same timer.

The MAR MODE trigger remains on until the indicators have been transferred at the last (IC) level and is reset by Indicator Transfer Timer $E.\overline{M} \cdot IC_i \cdot ABC_i$. (An additional trigger, MAR NEXT INSTRUCTION, set by the same sample which sets MAR MODE, is reset by Indicator Transfer Timer E·M only. This trigger essentially identifies ABC action on the first level of any instruction.)

In general, (store instructions excepted) the signal to gate in the indicators at the last level means the lookahead has entered its last indicator; therefore, the same sample is used to set the Lookahead Normal Indicator Test trigger.

The advance condition for the ABC is Indicator Transfer Timer-M and no interlock with the TBC. The SCC advances over this level on the basis of the tag bit combination LC·LF at the time the ABC interlock disappears.

1(b) Non-Store Operations (internal operands-Appendix IV p. 32)

The action of the TBC for levels involving internal operands is restricted to the Operation Code field gate out to the Execution Register. The necessary signals to begin pre-execution are the responsibility of the ABC; however, the previously described response, (To) provides the advance for the TBC in the usual manner.

The data and control paths involved to transfer the contents of an internal register to the C register are such that three cycles are required. Thus, the A-Timer is a three trigger timer, EE, E and M. The first trigger, EE is set by Indicator Transfer Timer E·M, the ABC decoding the INT

2. XF-XCZ-XVLZ-XVZ-XVGZ-XL-XE-XH

tag bit and the absence of ($NOOP_i$) and (NOOP MODE). Completion of the transfer (A-timer E• M) with the information at the C register input gates results in two pulses to the PAU; the previously described GI Op Code & Start signal and a new GI ACOB to C signal. The Advance Condition for the ABC is A-Timer M and no interlock, ABC-TBC. The interlock, however, prevents the advance until To is received and the TBC is allowed to advance. The SCC again advances over the level as soon as the SCC-ABC interlock disappears.

A Timer $E \cdot \overline{M}$ during an internal fetch transfer is used to 1) select a sample to reset the LAAR Busy trigger, thus allowing the Instruction Unit to enter another level requiring a Type III Enable signal, and 2) request the A Checker to Check Data for transfers involving other than addresses 7 and 11. (A special signal, No Check Data, accompanies these latter transfers since no check bits are involved.)

2) Store Operations (no fetch required-Appendix IV p. 38)

The previously described TBC action (non-internal operands) is identical for the single level store instruction. The ABC action, however, in addition to the transfer of Indicator and Instruction Counter fields described above, consists of effecting the transfer of the store data from the PAU to the appropriate destination.

The indication that the store data is available (latched on the Arithmetic Bus) following any PAU to-memory operation is the pulse, PAU Last Cycle Store. This pulse is remembered in the Last Cycle Store Memory trigger. A two cycle transfer is necessary here; thus, A-Timer-E trigger is set with Indicator Transfer E or M, Last Cycle Store Memory and the ABC decode line identifying the level. The data is gated into the proper destination by the sample selected by A-Timer E• M.

In order to properly sequence the interrupt system, the setting of Lookahead Normal Indicator Test trigger is delayed until A-Timer E• M for all store operations.

For stores directly to an internal register, the store is effectively completed by the ABC. Thus, the LAAR Busy trigger is reset by A-Timer $E \cdot \overline{M}$. Special signals are sent to the Arithmetic Checker controls for stores to the accumulator (GI A+B) such that residue will be updated. The ABC advances on A-Timer-M, no interlock ABC-TBC and the fact that the Indicator Register is not specified as the store address. In this special case, an additional timer (Indicator Register Timer) is used to time the transfer of the modified Index Result indicators from the Indicator Register to the Instruction Unit Updated Indicator Register (IR -- UIR) for local interrogation. The advance for this case is Indicator Register Timer M and no interlock.

For stores to external Memory or Index Core Storage, the LAAR Busy trigger is not reset until the SCC completes the store. Instead, A-Timer

$E \cdot \overline{M}$ resets the Store Check Test trigger, such that the interrupt mechanism will be interrogated after the SCC checks the data. To initiate this SCC action, the Level Filled tag bit is reset coincident with gating the data into the level.

To complete the instruction, the SCC action must be considered for each remaining memory area. An external store will be considered first. (Appendix IV p. 55)

The Op code becomes meaningful to the SCC decoder when the Level Filled tag bit is reset. Since the decode line cannot be guaranteed to be in its proper state until the second sample following this action, the SCC Late Decode Enable trigger is set by the first sample selected by the coincidence of $SCC_i \cdot LF_i \cdot LC_i$. This trigger is used to gate the decoder lines, to insure proper decoding.

The logic forming the request to the I Checker priority system consists of SCC Advance Enable Sequence, Late Decode Enable, the SCC decode line identifying the level, and the LAAR decode line identifying the memory area. Honoring of this request (1st priority) results in setting the E trigger of the Store Check timer which is used to time the transfer through the I Checker for check and check bit conversion to ECC. Store Check Timer $E \cdot \overline{M}$ resets the SCC Advance Enables sequence trigger disallowing any further request. The E trigger of the timer is used to gate the Operand field to the LAICIB, $E \cdot M$ times a pulse to the I Checker requesting a parity check on the word, while $E \cdot M$ selects the sample for gating the information back into the operand field. This last sample also sets the Store Check Test trigger to allow interrogation of the interrupt mechanism.

Coincident with the data gate-in, a self-resetting trigger, Lookahead Store Request is set and its output sent to the Memory Bus Control Unit. At the same time, the Gate Out LAMIB trigger is set to gate the information to the BCU. Upon receipt of the Lookahead Store Accept pulse from the BCU, the Store Data timer is set to time the information on the LAMIB. With $E \cdot M$ of this timer, Gate Out LAMIB is reset. $E \cdot \overline{M}$ selects the sample to reset the LAAR Busy trigger and set the Store Executed trigger to define the checking conditions for any subsequent forwarding of this data. The advance condition for the SCC is Store Data Timer-M and no interlock SCC-ABC.

An exception in this procedure exists when addresses 0 or 4 are specified. Since these are external memory locations and sources of zeros, the data is converted to zeros with ECC code and the store performed. This is accomplished by inhibiting both the gate out to the LAICIB and the request to check parity during the check cycle. This effectively puts zeros on the bus and the generated ECC is gated in after the check cycle.

The SCC action if the store address is Index Core Storage consists of a request (4th priority) to the I Checker Priority system for the lookahead to Instruction Unit transfer involved. Honoring this request sets the

LA-I timer. This timer has two memory (M) triggers: 1) M for Index Transfer which is used if the data destination is Index Core Storage and 2) M-for no Index Transfer for all other Lookahead to Instruction Unit transfers. The output of M for Index Transfer and the SCC decode line gates LAAR positions 13-17 and parity to the Index Address Bus.

The information is gated to the LAICIB with LA-I timer E and gated into the Instruction Unit X register by the sample selected by E• M for Index Transfer. This sample also sets the Store Check Test trigger and the Clear Index-E trigger. The timers, Clear Index and Write Index, time the transfer from the X register to the cores, Clear Index-E being used as a store request signal to the Index Core Storage controls. Clear Index E• M is used to reset LAAR Busy and set Store Executed, while the SCC advance condition is Write Index-M and no interlock SCC-ABC.

3) Fetch and Store Operations

The PAU fetch and store operations, (Add to Memory, Load Factor, etc.) are handled in two levels of lookahead. The first level buffers the Operation Code and fetch operand, while the second level is reserved to receive the store data. Each level is essentially handled independently by each counter.

The first level TBC action is identical to that previously described for single levels specifying internal or non-internal operands. This is also true of the ABC action with any variation being those functions performed on the basis of the IC tag bit--i.e.--gating into the Instruction Counter Buffer, setting the appropriate test trigger, and resetting the MAR MODE trigger.

Since the TBC function is not necessary at the second level, the decode line identifying this level serves as the counter advance condition directly. (For all levels other than first PAU levels, the TBC Late Decode Enable trigger is used to gate the output of the TBC decoder to insure proper decoding.)

The ABC and SCC action when the PAU indicates the store data is available (Last Cycle Store pulse) is identical to that described for single level store operations.

An alternate method of handling the store level exists when the instruction is not completed. An example of this is an attempt to perform the Divide Double operation when the Divisor Zero condition is indicated. The PAU then essentially rejects the instruction and replaces the Last Cycle Store pulse with a No Store Data pulse. This Store Inhibited Memory trigger remembers the condition until the ABC is prepared to act upon it. For convenience, the A-Timer is used only to select samples to perform the necessary cleaning-up functions necessary to proceed. These include resetting the LAAR Busy trigger and setting

the Lookahead Normal Test trigger. In addition, the NOOP tag bit is set at the level involved such that, should forwarding of the expected data have been specified in the interim between loading the store level and discovering the Divisor Zero condition, the Forward NOOP Conversion function will occur and allow the computer to continue.

4) Multi-fetch Operations

The final PAU instruction to be discussed is the Multiply and Add instruction. This involves two fetch operands as specified by the operand address and the (implied) contents of address 14. The first level again is identically handled with respect to transfer of the operation code and first operand and the initiation of pre-execution.

The second level contains the contents of the external core memory location 14. The TBC controls the transfer of the Operand field contents to the C register input gates. T-Timer $E \cdot \overline{M}$ times the signal PAU Continue and dwells until the information is accepted. The Cumulative Multiplier Accepted pulse sets the First Cycle Memory trigger such that the counter advances in the usual manner.

The overall lookahead timing chart[1] shows the non-synchronous counter action for a series of PAU instructions. Assumptions were made involving the speed of loading the lookahead, memory access times, and the PAU execution timing. Thus, this document is meant only to illustrate the lookahead action of sequencing the instructions.

B. SAU Instruction Execution

The SAU instruction set has been grouped into classifications similar to those of PAU instructions with respect to fetch functions and store functions. Four general classifications exist:

1. Non-store operations
2. Fetch and Store Operations

This category includes the normal add-to-memory type operations where the number of stores involved equals the number of fetches.

3. Fetch and Special Store Operations

This category includes the Load Factor type operations where, regardless of the word boundary crossover considerations of the fetch operand, only a single store operation is necessary.

4. Multiply and Add Operation

1. Appendix IV-p. 59

Figure 1 shows the sequence of levels encountered in handling each category under the various WBC and progressive indexing (PX) conditions. With the exception of the special fetch operand of the multiply and add instruction, all fetch operands may specify the contents of an internal register.

As evidenced by Appendix IV, the information transfer and instruction sequencing functions are very similar to those encountered for PAU instructions; therefore, only the major variations will be presented here.

SAU Op Code Level (Appendix IV-p. 1)

This level is identified by the coincidence of $LAOP_i \cdot OP9_i$. The gate out of the Operation Code field, Operand field and WBC tag bit to the input gates of the SAU execution register is accomplished by the usual decode method. The trigger, SAU START is set with the sample selected by T-timer $E \cdot \overline{M}$ and establishes a d.c. signal to the SAU controls. (The trigger output is ORed with its set condition such that the SAU may act upon it coincident with the arrival of the data.) The TBC dwells until the d.c. reply, SAU Housekeeping, is received indicating data acceptance. The sample selected by SAU START-SAU Housekeeping resets the Start trigger and sets First Cycle Memory to effect the TBC advance.

SAU Operand Levels (Appendix IV-pp. 2-11)

Once the SAU is in the housekeeping state, the C and D registers are available to receive the necessary operand or operands. Thus, the lookahead controls the entire transfer including the data gate in signals.

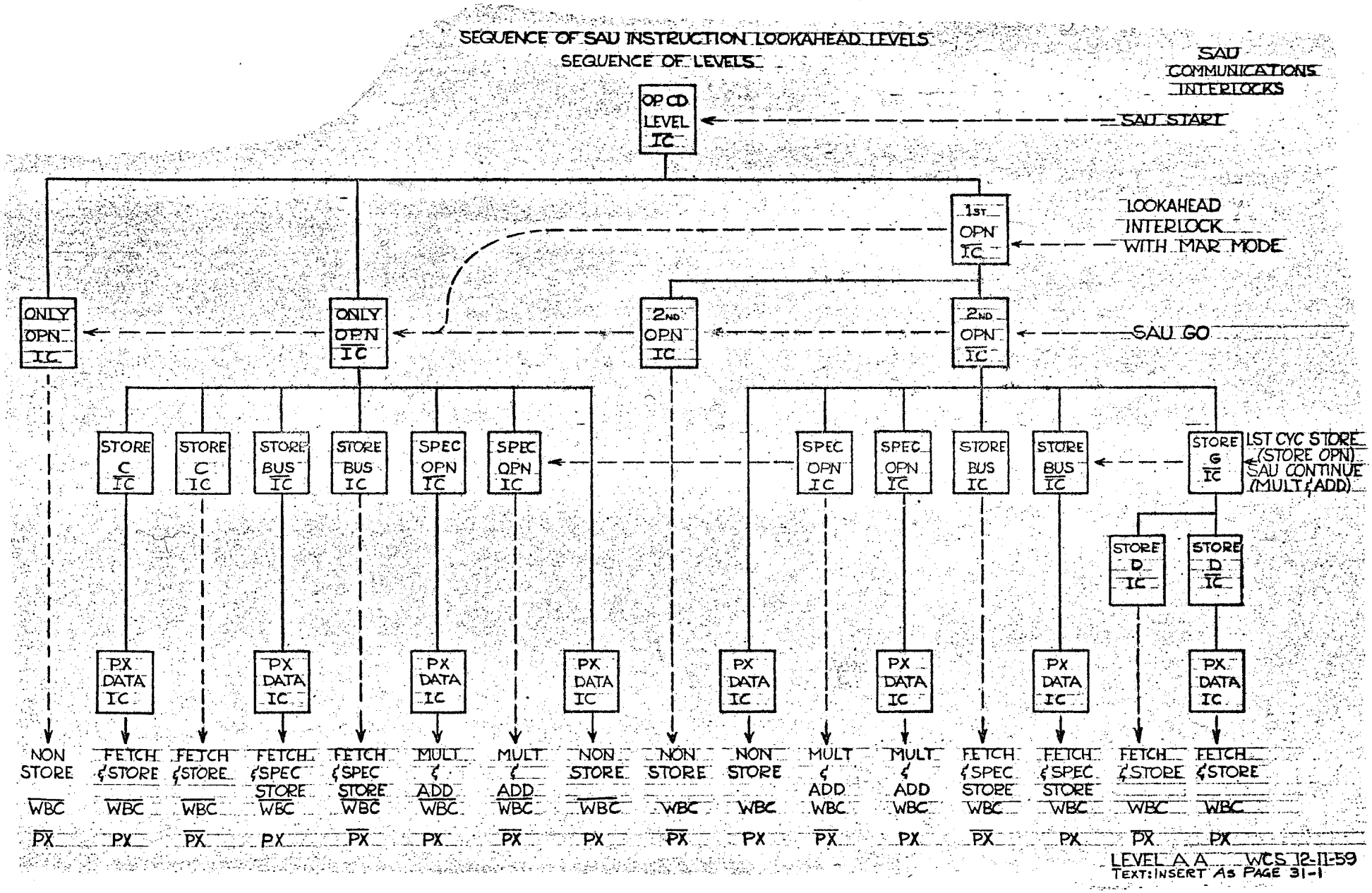
The operand destinations are defined as the C register for single (only) operands and the first of two operands, and the D register for the second of two operands. (Excluding the special operand of Multiply and Add, in which case the destination is again the C register.)

Completion of the last operand transfer results in a signal, SAU GO, which allows the SAU to terminate the housekeeping state and begin instruction execution. Since the SAU contains no equipment to interrogate the interrupt mechanism, the GO signal indicates:

1. That the necessary operands are in the CD registers and
2. That the previous instruction caused no program interrupt.

The transfer of non-internal operands is the responsibility of the TBC.

To satisfy the second condition above, the set of T-timer E is dependent upon the presence of MAR MODE conditions during transfers of the first (or only) SAU operand. The SAU GO trigger is set with T-timer $E \cdot \overline{M}$,


SEQUENCE OF SAU INSTRUCTION LOOKAHEAD LEVELS
SEQUENCE OF LEVELS
SAU COMMUNICATIONS INTERLOCKS
OP CD LEVEL IC
SAU START
1ST OPN IC
LOOKAHEAD INTERLOCK WITH MAR MODE
ONLY OPN IC
ONLY OPN IC
2ND OPN IC
2ND OPN IC
SAU GO
STORE C IC
STORE C IC
STORE BUS IC
STORE BUS IC
SPEC OPN IC
SPEC OPN IC
SPEC OPN IC
SPEC OPN IC
STORE BUS IC
STORE BUS IC
STORE G IC
1ST CYC STORE (STORE OPN) SAU CONTINUE (MULT & ADD)
STORE D IC
STORE D IC
PX DATA IC
NON STORE
FETCH & STORE
FETCH & STORE
FETCH & SPEC STORE
FETCH & SPEC STORE
MULT & ADD
MULT & ADD
NON STORE
NON STORE
NON STORE
MULT & ADD
MULT & ADD
FETCH & SPEC STORE
FETCH & SPEC STORE
FETCH & STORE
FETCH & STORE
WBC
PX
LEVEL A A
WCS 12-11-59
TEXT: INSERT AS PAGE 31-1

and its output "or" set condition establishes the d.c. signal to the SAU controls. The trigger is reset by SAU GO·NO SAU Housekeeping. T-timer M and no interlock TBC-OCC serves as the TBC advance condition.

The ABC control of internal operand transfers is similar to that previously discussed with the SAU GO trigger set, when applicable, with A-timer E-M. (The TBC, when an internal register is specified as an SAU operand, has no function to perform. However, to facilitate handling SAU instructions under program interrupt conditions, the counter is not allowed to advance until an interlock is established with the ABC. The ABC decode line in this case serves as the TBC advance condition after A-timer E-$\overline{M}$ is used to reset the TBC Advance Enables Sequence trigger.)

SAU Store Levels (Appendix IV pp. 12-19)

The levels reserved to receive SAU store information fall into three categories:

1. Store C level - receives information from the C register following Fetch and Store operations. The result is gated from C for "only" store ($\overline{WBC}$) and first of two stores (WBC).

2. Store D level - receives the second word from the D register following Fetch and Store operations specifying Word boundary crossover.

3. Store bus level - receives store data following Fetch and Special Store operations. Following this class of SAU instructions, the data is latched on the Arithmetic Checker bus.

The ABC and SCC action here following receipt of the Last Cycle Store signal indicating data availability is similar to that previously described. The data and control paths involved for transfers from the C and D registers (as opposed to transfers with the data already latched on the ACIB) are such that the A-timer EE trigger is used to allow a three cycle transfer.

Although the TBC has no action at these levels, the ABC interlock is formed to prevent the advance until the C and D registers are clear.

SAU Special Operand Levels (Appendix IV pp. 20-21)

The special operand for the SAU multiply and add instruction poses the same interlock problem as its PAU counterpart in that the destination of the data is the same (C) register as that used to buffer an "earlier" operand. Therefore, the TBC action is inhibited until the pulse SAU Ready for MPYC Operand is received. This again sets a Memory trigger and T-timer E is set to time the transfer. The gate out of the Operand field is the TBC d.c. decode line identifying the level and the data is gated in to C with the sample selected by T-timer $E \cdot \overline{M}$. The memory trigger is reset by this same sample, and its absence serves as the indication to the SAU that the operand is available.

SAU Progressive Indexing (PX) levels. (Appendix IV-p. 22)

The final level of all SAU instructions in which the progressive mode of indexing is specified is used to buffer the original contents of the affected index core storage loca tion. During normal operation, the only lookahead functions required are the transfer of indicators and instruction counter fields at the ABC level. Since the progressive indexing function allows the index result indicator to change, this category of indicators is included in the transfer.

Special SAU Instructions:

The Branch on Indicator and Branch on Bit instructions are treated as special SAU instructions since, for economy reasons, the SAU equipment is utilized to perform the bit testing and modification necessary. These instructions therefore require lookahead action similar to other SAU instructions.

The Instruction Unit assumes the test will fail and continues to process instructions accordingly. A special (branch recovery) level following those necessary for processing the SAU action buffers the Branch Address such that, upon detecting that the branch is to take place, a modified housecleaning procedure will allow the Instruction Unit to recover.

The Instruction Unit preparation of these instructions include testing for those conditions which, if the branch conditions are met, cause the instruction to be rejected. These include the branch address failing the address invalid (AD) or instruction fetch (IF) tests, certain store addresses failing the Data Store (DS) test, and the instruction itself failing the Execute Exception (EXE) test. These conditional indicators must be interrogated by the SAU such that the presence of any one serves to inhibit the bit modification when the branch conditions are met. For this purpose they are buffered in the Operation Code field of the first level associated with these instructions. Normal TBC action places

them in the SAU execution register.

Branch on Bit (BB)[1]

Lookahead processing of the three SAU levels involved is similar to the add-to-memory operation specifying a single operand. The TBC decode line identifying the first level of these special instructions is memorized by the SAU and serves to identify the instruction, in lieu of any SAU Op Code.

Coincident with the Last Cycle Store pulse, responses indicating the results of the bit test and the status of the conditional indicators are memorized by the lookahead in the Branch Test Result triggers to define the action to be taken at the branch recovery level.

The ABC action at the recovery level, in addition to the normal transfer of indicators, etc., varies depending upon the response.

1. Branch Unsuccessful

   No special action since Instruction Unit assumption was correct and the instruction was not rejected.

2. Branch Successful-conditional indicators

   Instruction Unit assumption was correct (since instruction is rejected) and the conditional indicators are entered into the Indicator Register. This is a direct path from the SAU Execution register to the input gates of the Indicator Register.

3. Branch Successful-no conditional indicators

   This case indicates the Instruction Unit assumption was incorrect and any later lookahead levels must be considered invalid. Thus, the housecleaning Mode of operation is initiated in order to recover.

(The Housecleaning Mode of operation may be entered due to any one of three conditions occurring. The action is discussed in a later section of this memo.)

Branch on Indicator[2]

The associated fetch and store levels of the Branch on Indicator instruction are distinctly coded due to special handling of bit positions 0-19 of the Indicator Register. These bit positions are normally unaffected by the storing function; however, to accomplish the bit resetting function of this instruction, coincident with the transfer of the register contents to the C register, bits 0-19

1. Appendix IV-pp. 27, 4, 13, 28
2. Appendix IV-pp. 24, 25, 26, 28

are reset. There is then a unipolar gate provided and activated by the ABC during the store transfer.

With this exception, the Branch on Indicator and Branch on Bit instructions are handled identically by the lookahead.

Store Instruction Counter if Branch on Indicator [1]

A variation of the Branch on Indicator instruction is encountered when prefixed with the Store Instruction Counter If function. In this case an additional level of lookahead is involved. This additional level requires different action depending upon the branch conditions.

No assumption is made concerning the success of the bit test. Instead after loading the recovery level into the lookahead, the Instruction Unit waits for the SAU to complete the test before completing the instruction. (Since the Instruction Unit retains the branch address in this case, no recovery is necessary and the "recovery level" exists only for control simplicity).

The special action of the ABC at the recovery level is modified to the following: (The coding of this level differs from the recovery load for Branch on Indicator/Bit only by the absence of the IC bit.)

1. Branch Unsuccessful

   In addition to the transfer of indicators, the control pulse, Resume-No Stica is sent to the Instruction Unit. The additional level in this case is a "dummy" level with the IC tag bit to effectively close out the instruction and cause the interrupt mechanism to be memorized.[2]

2. Branch Successful-conditional indicators

   Same as 1) above with these indicators entered into the Indicator Register.

3. Branch Successful-no conditional indicators

   In this case, the control pulse Resume-Stica is given the Instruction Unit. This unit proceeds to effect the store instruction counter action and places the result in the lookahead for eventual storing.

   (The action at this final level is similar to that of other Instruction Unit store type instructions and is discussed in that section of this memo.)

1. Appendix IV-pp. 24, 25, 26, 30
2. Appendix IV-p. 45

C. Non-Arithmetic Instruction Execution

Execution of instructions which involve neither arithmetic unit differs somewhat from the previously described action for sequencing the Interrupt Mechanism. These instructions include the Input-Output class and those executed directly by the Instruction Unit.

The Noop Indicator Test trigger is used to indicate the last indicator setting. In addition, the PAU contains a Master Tests Complete trigger which is functionally the PAU counterpart of the lookahead MAR MODE trigger and must be reset between each instruction. This action is the responsibility of the lookahead for all non-arithmetic instructions and is accomplished at the last level with the sample selected by Indicator Transfer $E \cdot M, IC_i$, ABC_i and the ABC decode line identifying these type instructions

It should be noted that, though the TBC has no action to perform at many of the levels to be described here, the advanced must be delayed until the above action has been accomplished to eliminate the possibility of the PAU falsely interrogating the Master Tests Complete condition. At these levels, the ABC decode line serves as the TBC advance condition after Indicator Transfer $E\text{-}\overline{M}$ is used to reset TBC Advance Enables Sequence trigger.

1. Input-Output Instructions[1]

The location of the information required by the Exchange Units for execution of I/O instructions is shown in the Operand and Operation Code field format documents in Appendix II. This information includes the Control Word Address, Unit Address and Operation Code. In addition, the Instruction Unit determines the proper Exchange Unit involved and sets Op Code position 7 accordingly.

The transfer of this information is the responsibility of the TBC and takes place via the TOB. The level is identified by coincidence of $\overline{LAOP_i}$, $\overline{OP\text{-}9_i}$, $\overline{OP\text{-}8_i}$, TBC_i and the gate out to the TOB takes place in the usual decode manner. Prior to selecting the Exchange, however, all previous storing functions are concluded. In addition, no select is given if an interrupt occurs. Thus, T-timer E is delayed until the MAR conditions have been met and the interlock show the SCC to be at the same level.

T-timer M and the TBC decode line identifying the proper Exchange establishes the d.c. Select Basic Exchange or Select High Speed Exchange signals. No further action

1. Appendix IV-pp. 49-51

occurs until the instruction has been accepted or rejected.

When the Exchange accepts the instruction, the accept pulse is remembered in the I/O Reaction Storage trigger and, after proper clock pulse synchronization, the I/O response trigger serves to advance the TBC.

When the Exchange rejects the instruction, this signal is sent to the Interrupt Mechanism controls to record the proper I/O reject indicator. This reject signal is then relayed to the lookahead and performs essentially the same action in establishing the TBC advance condition. In either case, the accept or reject signal resets T-timer M directly to terminate the Select signal.

The second level provided for I/O instructions is a dummy level tagged with the IC bit such that the interrupt mechanism is interrogated.

2. Instruction Unit Instructions

The instructions executed within the Instruction Unit are generally completed within that unit to the point where it is necessary to store and/or enter indicators. These functions are completed by the lookahead in proper sequence. These levels are referred to as:

(1) Instruction Unit Store levels
(2) Indicator Transfer Only levels

Two other levels exist to process the cases where Index Core Storage is modified and where the lookahead must furnish the contents of an internal register for proper execution by the Instruction Unit. These levels are referred to as:

(3) Pseudo Store level
(4) Internal Fetch level

Proper combinations of these four types of levels provide the lookahead action necessary for completion of all Instruction Unit instructions. Appendix III shows specifically the type level or levels involved for each instruction.

It should be noted that those instructions which the Instruction Unit terminates by loading the lookahead with any of the first three levels above may cause the Index Result indicators to change; thus, this category of indicators is included in the transfer.

(1) Instruction Unit Store Levels

In general, these levels may specify either external memory locations or an internal computer register as indicated by the contents of the LAAR. When external memory is specified, the necessary ECC bits, if possible, are generated during the loading process, thus eliminating the necessity of the SCC check and check bit conversion cycle. The WBC tag bit is set by the Instruction Unit and used in conjunction with this particular Lookahead Operation Code to identify this condition.

a. External Store in ECC[1]

The ABC at this level, coincident with Indicator Transfer timer E-$\overline{M}$ resets the LF tag bit to initiate SCC action. This latter action provides the store request to the BCU directly, followed by the previously defined sequence of operations necessary to effect the transfer of the information to the BCU. (The level at which the store is effected following the Store Instruction Counter if Branch on Indicator instruction is handled in this manner.[2] However the Index Result indicators do not apply and since the SAU is involved, the Lookahead Normal Test trigger is used.

b. External Store in Lookahead Parity[3]

It is not always possible, for checking purposes, to include the generation of ECC during the loading process. Thus, the necessity may exist for the normal SCC check cycle. The absence of the WBC tag bit indicates this condition and the ABC, coincident with Indicator Transfer timer E-M, resets the Store Check Test trigger. The SCC action is identical to that previously described with the Interrupt Mechanism interrogated after the check and check bit conversion cycle.

1. Appendix IV-p. 41-42-57
2. Appendix IV-p. 43
3. Appendix IV-p. 41-42-55

c. Internal Store[4]

The date path existing for effecting the transfer of store data from a lookahead level to an internal register exists only through the C register. Thus, the function is performed in two steps, the TBC controlling the transfer from the Operand field to C and the ABC completing the transfer from C to the internal register specified by the LAAR contents. T-Bus timer E is set after an interlock is established with the ABC and after the MAR MODE conditions are met. The TBC is not allowed to advance until ABC completes the store, the advance condition being A-timer M and no interlock. Use of A-timer EE provides the necessary three cycle transfer from C. This trigger is set by T-timer M, Indicator Transfer M and the ABC decode line identifying the level. The remaining action is similar to that described previously.

(2) Indicator Transfer Only Level[1]

Processing the Indicator Transfer Only Level entails only the indicator transfer function and interrupt sequencing action.

(3) Pseudo Store Level[2]

During normal operations, this level is identical to 2) above. Only in the event of rejecting the instruction or detecting a program interrupt do the Operand field contents become useful information.

(4) Internal Fetch Level[3]

The lookahead action of supplying the contents of an internal register to be used as an Instruction Unit operand is accomplished in two steps. The transfer from the specified internal register to the Operand field is accomplished at the ABC level. This takes place subsequent to the transfer of indicators and is timed by the A-timer in the usual manner. The sample selected by A-timer E-$\overline{M}$ resets LF to allow completion of the transfer by the SCC.

4. Appendix IV-p. 39-40
1. Appendix IV-p. 44
2. Appendix IV-p. 46, 47
3. Appendix IV-p. 48

The SCC decode line identifying the level participates in the request to the I checker priority system. When priority has been established, the LA to I timer E trigger is set. (M for no Index Transfer is used here.) The information is gated to the LAICIB with this trigger and the signal given to gate in the data to a pre-selected Y register. The LA to I memory trigger serves to advance the SCC on the first sample following the disappearance of the interlock.

VIII Instruction Reject Control Definition

The action described to this point allows processing the entire computer instruction set under normal operating conditions. It is possible, upon detection of certain conditions during preparation, to reject the instruction. These conditions cause the No Op tag bit to be set in the level involved and include:

1) Abnormalties detected during the Instruction Unit preparation, prior to loading the lookahead, such as addresses failing the boundary comparison circuits, invalid operation codes, errors, etc.

2) An operand address failing the Memory checking circuits.

3) The operand itself failing the I-Checker circuits.

Under control of the No Op bit, normal functions are inhibited and only the necessary interrupt system sequencing functions are performed. The presence of this bit at any level through the last (fetch) operand level associated with a given instruction causes the entire instruction to be rejected. Beyond this point, the No Op bit will not appear since the execution units are allowed to modify addressable registers.

During the ABC action (Transfer Indicators $E \cdot \overline{M}$) at a No Oped level, the No Op MODE trigger is set and remains on to define the action through the last level associated with the instruction.

TBC action consists of merely advancing over a rejected instruction on the basis of No Op MODE$\cdot \overline{IC_i} \cdot TBC_i$. At the last level, no action occurs until the ABC has completed action at this same level, at which time the TBC advance into the next instruction and the No Op MODE trigger reset occur simultaneously.

The ABC action during instruction rejection includes the transfer of the Instruction Exception and the CNIDC indicators, with the No Op Indicator Test trigger recording the last transfer. In addition, upon detecting a store level during this mode of operation, the LAAR Busy trigger is reset and the No Op tag bit set. Thus, if necessary, the Forward No Op Conversion cycle may take place to allow the computer to continue.

PAU Instruction Reject

In general, the PAU is not allowed to begin pre-execution of an instruction to be rejected. The exception occurs when the special operand associated with the PAU Multiply and ADD instruction is No Oped. In this case, the PAU MPYC Reject pulse is given in lieu of the PAU Continue signal, and the instruction terminated prior to modifying an addressable register.

SAU Instruction Reject

The d.c. output of the SAU Reject trigger serves to cause rejection of SAU instruction. This signal is given only when housekeeping has actually begun and is given only at the first No Oped operand level. The SAU Enabled Memory trigger set by the ABC (Indicator Transfer E• M) at the first SAU level (if not rejected) remembers the first condition above. The logic for setting SAU Reject is, then, SAU Enabled Memory, No Opi, ABC_i, No No Op MODE, Indicator Transfer $E \cdot \overline{M}$. The trigger is reset by the SAU NOT OPERATING condition indicating instruction rejection prior to the modification of an addressable register. The SAU Enabled Memory trigger is reset at the last level with the sample selected by Indicator Transfer E• M, ABC_i, IC_i.

Pseudo Interrupt

Four levels exist which normally cause the Index Result indicators to be changed. These are:

1) Instruction Unit Store level
2) Indicator Transfer Only level
3) Instruction Unit Pseudo Store level
4) SAU-PX Pseudo Store level

When an instruction resulting in any of the above levels is rejected, the transfer of these indicators is inhibited at the ABC level; thus, the Instruction Unit record of these indicators is in error. The validity of any subsequent levels appearing in the lookahead is in question and House-cleaning action is initiated to recover. This recovery is referred to as a "pseudo interrupt".

Following this action, the applicable bit positions of the Indicator Register are transferred "back" to correct the Instruction Unit Updated Indicator Register, the contents of the IC Buffer are transferred to the Instruction Counter and the Instruction Unit resumes by re-preparing instructions from this point.

No Op Code

The interpretation placed on the No Op tag bit prohibits the bit setting beyond the last fetch operand level of SAU instructions. However, errors detected during the loading of 1) pseudo store data for the progressive

indexing level and 2) the branch address into the branch recovery level must be recorded and appropriate action taken. Only if this recovery data is to be used is this error significant. The error line is gated into Operation Code position 8 and the CNIDC indicator. The former action converts these particular Lookahead Operation Codes to "No Op Codes" and the level is handled consistent with instruction reject action. When it is determined a recovery is necessary, the CNIDC indicator is transferred to the MK position of the Indicator Register.

IX Lookahead Housecleaning Mode of Operation

The Housecleaning mode of operation may be necessitated by any of three conditions:

1. Detection of program interrupt,
2. Detection of the need for "pseudo interrupt",
3. Detection of the need for "branch recovery".

In each case, the levels beyond that at which the ABC initiates the Housecleaning mode are considered invalid. Lookahead loading is terminated immediately and, at any level containing pseudo store data, the operand field is transferred to Index Core Storage to "back date" this memory area. This action continues until all counters are interlocked with the IAUC and the IAUC Advance Enables Sequence trigger is on indicating all levels have been processed. The necessary lookahead status triggers are then reset to allow resumption of normal action before allowing the loading to begin.

A. Housecleaning due to an interrupt

This action is initiated due to the Interrupt Next Instruction trigger indicating the latest memorization of the interrupt line. The sample selected by this trigger, ABC Advance Enables Sequence, $ABC_i \cdot LF_i \cdot LC_i$ sets E trigger of the Houseclean Timer which is used (in place of the Indicator Transfer timer) throughout the remaining levels during this mode of operation. At this time, synchronization with the Instruction and Execution Units occurs to define the status of the computer. Appendix II contains, in flow chart form, a description of the Execution States.

The sample selected by Houseclean Timer E·M·No LA Houseclean Mode. Interrupt Next Instruction: 1) sets the Interrupt Inhibits Load trigger the output of which inhibits all Load Enable signals to the Instruction Unit.-2) sets the LA Disable Interrupt trigger which insures the memorization of no new interrupt until this recovery is complete. -3) sets the I Houseclean Request trigger informing the Instruction Unit of the recovery. This trigger is reset by that unit upon initiation of that action necessary to insure availability of the registers necessary to receive recovery data from the lookahead. Completion of this action is indicated by the d.c. signal LA Houseclean Request from the Instruction Unit.

When the instruction at this level-i.e., the instruction being interrupted-is the first level of a PAU instruction (specifying a non-internal operand and is not rejected), it is evident that the PAU will begin pre-execution. This units action upon detection of the interrupt condition, is to terminate pre-execution and enter an "Idle" state such that no further instructions may begin. (This is necessary since it cannot be guaranteed that the TBC has not given the GI Op Code & Start signal which applies to the next instruction. Neither the PAU nor the SAU may honor a Start signal from the lookahead while the PAU is in this "Idle" state.)

The pulse, Set Execution Units Idle from the PAU indicates this condition and is sampled into the Execution Unit Idle trigger. Coincidence of this trigger and Lookahead Houseclean Request sets the LA Houseclean Mode trigger which controls the action at the remaining levels of lookahead.

When the interrupted instruction is the first level of an SAU instruction (not rejected), it is evident the SAU will begin its Housekeeping activity. This ABC decode line, Houseclean Timer E·M, and No LA Houseclean Mode sets SAU Instruction Interrupt as temporary storage. This trigger and SAU Housekeeping sets the SAU Reject trigger which again informs that unit to terminate prior to modification of an addressable register. SAU Not Operating·SAU Reject·Interrupt Inhibits Load·SAU Instruction Interrupt is used to set Execution Units Idle.

When the ABC decodes any level other than the first level of PAU or SAU instructions, the Execution Units Idle trigger is set directly (Houseclean Timer E·M) by the lookahead such that the LA Houseclean Mode trigger will be set in the usual manner after the Instruction Unit completes the necessary recovery.

By this method, then, once LA Houseclean Mode is present, the state of all other units involved has been established and the lookahead may proceed to restore any necessary data. (It should be noted that LA Houseclean Mode inhibits normal TBC action, so until this trigger comes on, the TBC continues to function normally. This should justify the concept of the necessary execution units "idle" state.

The LA Houseclean Mode provides a continuous advance condition for the TBC such that this counter will advance through to the IAUC level contingent only upon the TBC-OCC interlock. At each level to be housecleaned, the ABC action is restricted to:

1) Transfer only the CNIDC indicator to the Indicator Register to record errors in recovery information.

2) Reset LAAR Busy and set the No Op tag bit at levels requiring use of the LAAR. (This again allows the Forward No Op Conversion Cycle if forwarding has been specified.) This action is performed by the sample selected by LAAR Busy, ABC_i, $From_i$, Houseclean Timer $E \cdot M$.

3) Resetting the LF tag bit in pseudo store levels to allow the SCC to return the index word. This is done with the ABC decode line and Houseclean Timer $E \cdot \overline{M}$.

The advance condition of the ABC during housecleaning is Houseclean Timer M, LA Houseclean Mode and no interlock ABC-TBC.

The SCC action of returning the index word[1] is contingent upon LA Houseclean Mode and is very similar to effecting a valid store to Index Core Storage. The address involved, however, is buffered in positions 1-4 of the Operation Code Field.

The process of returning this recovery information must be accomplished in "reverse" order--i.e.--the "earliest" original contents of any one Index Core Storage location is the only information to be restored. Thus, during the return of data, the address involved is compared with all other pseudo store addresses in lookahead and the comparison signal gated into Operation Code position O of the level compared with. This new lookahead Operation Code is then interpreted by the SCC as merely an advance condition.

The ABC and SCC action continues until all counters indicate the same (IAUC) value indicating the lookahead is empty. With the sample selected by $IAUC_i$, OCC_i, TBC_i, ABC_i, SCC_i, IAUC Advance Enables Sequence, and LA Houseclean Mode, the Houseclean Over Timer is used to reset the various computer status triggers to allow resumption of normal action.

Houseclean Over $E\ \overline{M}$ selects a sample to:

1) Gate the contents of the IC Buffer to the Instruction Counter. This is a direct path.

2) Gate the Index Result indicator position of the Indicator Register to the Instruction Unit Updated Indicator Register. This corrects the latter information for local interrogation.

3) Reset the PAU and SAU Start triggers. This removes the false start which may have been set up by the TBC before LA Houseclean Mode terminated this counters normal action.

1. Appendix IV-p. 58

4) Reset lookahead MAR MODE and the PAU Master Tests Complete triggers in preparation for re-memorizing the interrupt line.

5) Reset LA Houseclean Mode and Interrupt Inhibit Load triggers to allow further lookahead loading. (This sample also resets Pseudo Interrupt Inhibits Load and Branch Recovery Inhibits Load used during these types of housecleaning action.)

Houseclean Over E·M selects a sample to:

1) Set the PAU Wait trigger. This essentially terminates the PAU "Idles" state allowing this unit to accept new instructions.

2) Set the No Op Indicator Test trigger which allows re-memorization of the interrupt line in the usual manner. Since the LA Disable Interrupt trigger is on, this memorization results in MAR MODE and MAR Next Instruction.

Houseclean Over Timer-M forms a d.c. signal to the Instruction Unit to resume. The first action includes "generating" a special Branch on Indicator instruction (IRPT-BIN) to accomplish resetting the bit which caused the interrupt. The conditions, branch if bit is off (F/N) and set to zero (L/Z) are generated. Thus the SAU accomplishes the bit resetting and the lookahead action is identical to that of the Branch on Indicator instruction with the Branch Unsuccessful response. (The TBC decode line at the first level[1] is memorized by the SAU in lieu of any SAU op code.)

The next instruction seen by the lookahead is the "free" instruction stored at the address specified by the sum of the Interrupt Address and the bit address of the bit causing the interrupt.

The LA Disable Interrupt trigger is reset by MAR Next Instruction, Indicator Transfer timer E·M and inhibited by the ABC decode line identifying the first level of the IRPT-BIN instruction. In this manner, it is insured that both the IRPT-BIN instruction and the free instruction will be executed by the lookahead before a new interrupt may be honored.

(An additional Interrupt Test level exists for the special purpose of forcing interrogation of the interrupt mechanism. In certain cases, (notably the Transmit or Swap instructions) it is desirable for the Instruction Unit to complete stores to the Index Core Storage area without recourse to loading successive pseudo store levels since the depth of lookahead limits the degree of recovery possible. This may be accomplished only upon proving logically that the instruction is not to be interrupted.

Prior to taking this action, an Interrupt Test level is loaded into the lookahead, after which the Instruction Unit waits for the Lookahead

1. Appendix IV-p. 54

Empty signa. This signal is formed by MAR MODE, + IRPT NEXT INSTRUCTION, No Forward Required, the absence of all Inhibit Load triggers, all counters interlocked, IAUC Advance Enables Sequence, and the fact that the level designated by the IAUC is not disconnected.

The normal action[1] taken at this level is seen to be similar to that of the Indicator Transfer Only level with the Index Result indicators unaffected.)

B. Housecleaning due to Pseudo Interrupt

This action is necessary upon detection of a rejected instruction affecting the Index Result indicators. The action is initiated during ABC action at the last (IC) level of the rejected instruction, thus insuring the address of the next instruction appears in the IC Buffer.

The sample selected by the ABC decode line, and Transfer Indicators $E \cdot \overline{M}$ sets the Pseudo Interrupt Inhibits Load and the I Houseclean Request triggers. Following the Instruction Unit recovery, the sample selected by LA Houseclean Request, Pseudo Interrupt Inhibits Load and No LA Houseclean Mode sets LA Houseclean Mode.

The lookahead action once the Mode trigger is on is identical to that previously described. The Instruction Unit resumes, however, by merely re-preparing the instruction specified by the contents of the IC Buffer. (The Inhibit Load triggers serve as memory of the particular type of housecleaning action and define the method of resumption necessary for the Instruction Unit.)

C. Housecleaning due to a Branch Recovery

This action is necessary upon detection of the Instruction Unit making a false assumption in attempting to process the Branch on Bit/Indicator instructions. The action is initiated by the ABC at the branch recovery level associated with these instructions.

The Branch Recovery Inhibits Load trigger terminates the loading process, and the I Houseclean Request signal is given. LA Houseclean Request from the Instruction Unit, Branch Recovery Inhibits Load and No LA Houseclean Mode sets the LA Houseclean Mode trigger. SCC action of returning the branch address[2] is contingent upon this Mode trigger (since LF was reset by the ABC "early".) The LA to I timer is used to time the transfer with the data destination of a preselected Y register.

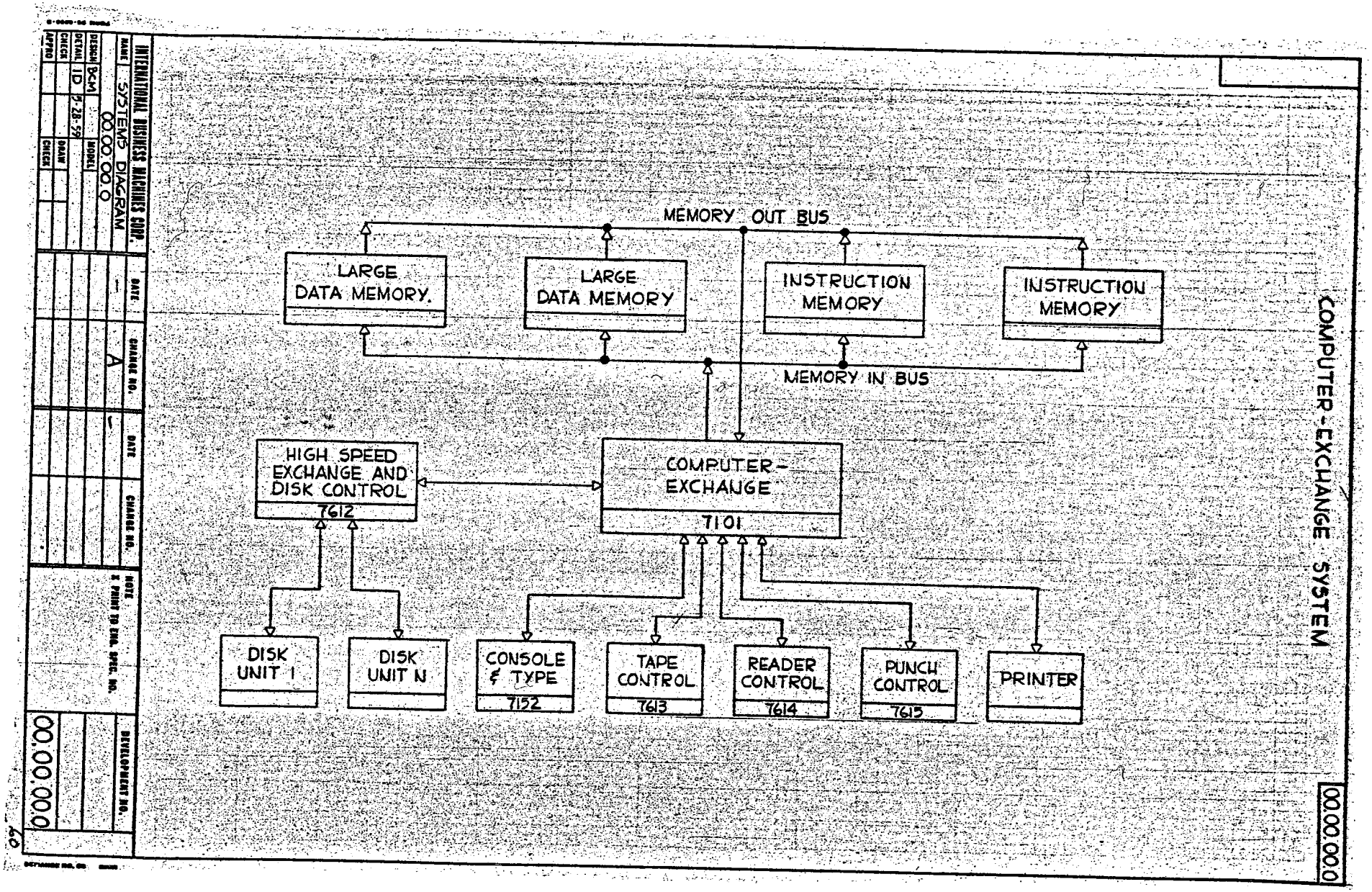
1. Appendix IV-pp. 52-53
2. Appendix IV-p. 56

The recovery at the remaining levels is identical to that for housecleaning due to a "real" interrupt or pseudo interrupt. However, upon completion of this recovery, the Instruction Unit resumes by preparing the instruction specified by the Branch Address and continues from this point.

Regardless of the type of recovery, the reset accomplished with Houseclean Over Timer essentially allows normal lookahead action to continue when the Instruction Unit resumes the loading process.

X Appendix

Appendix I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DISK UNIT 1
DISK UNIT N
CONSOLE & TYPE
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TAPE CONTROL
7613
READER CONTROL
7614
PUNCH CONTROL
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INTERNATIONAL BUSINESS MACHINES CORP.
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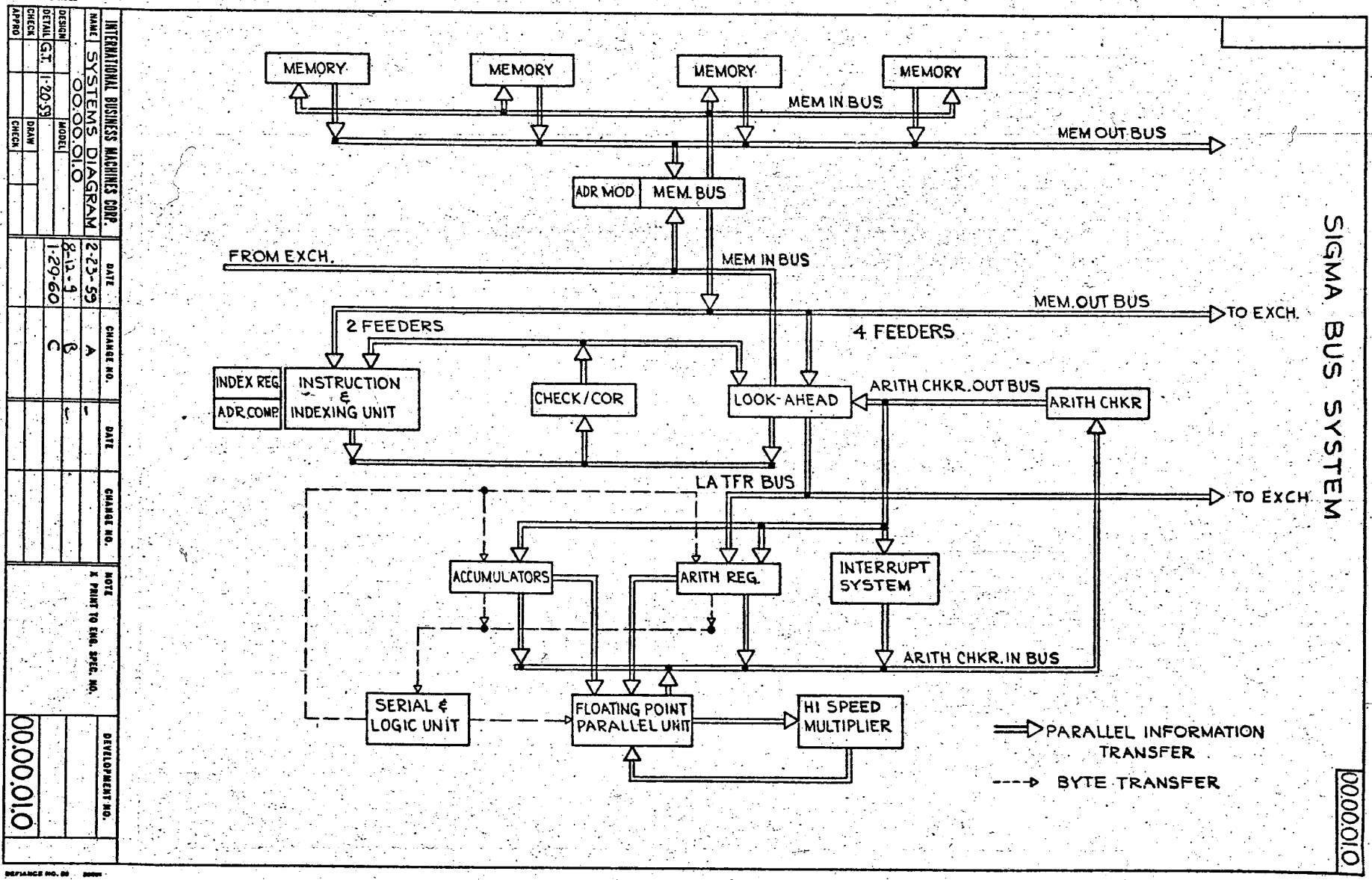
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2 FEEDERS
4 FEEDERS
INDEX REG.
ADR. COMP.
INSTRUCTION & INDEXING UNIT
CHECK/COR
LOOK-AHEAD
ARITH CHKR. OUT BUS
ARITH CHKR
LA TFR BUS
TO EXCH.
ACCUMULATORS
ARITH REG.
INTERRUPT SYSTEM
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FLOATING POINT PARALLEL UNIT
HI SPEED MULTIPLIER
PARALLEL INFORMATION TRANSFER
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DWG. SIZE - B

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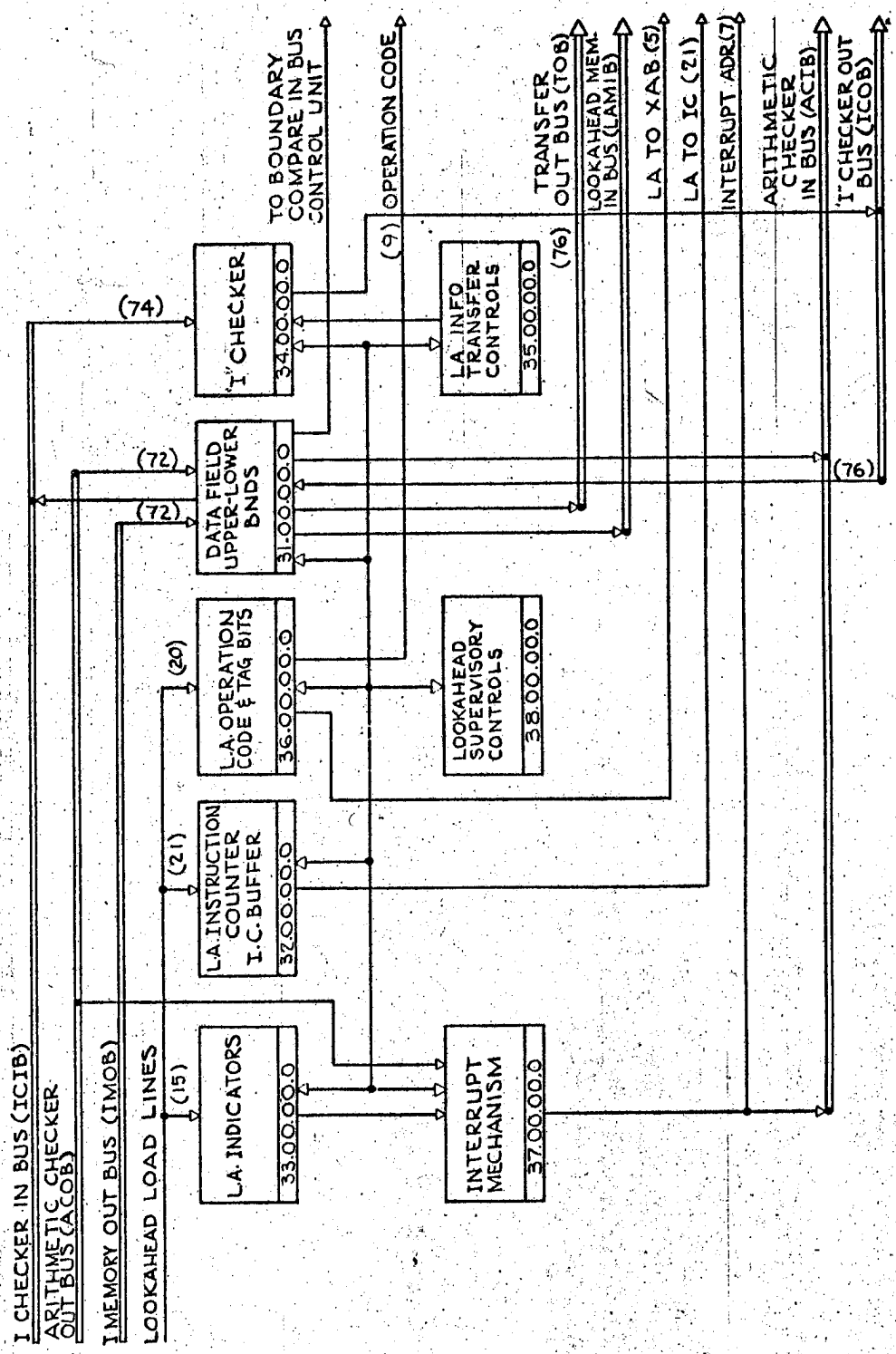

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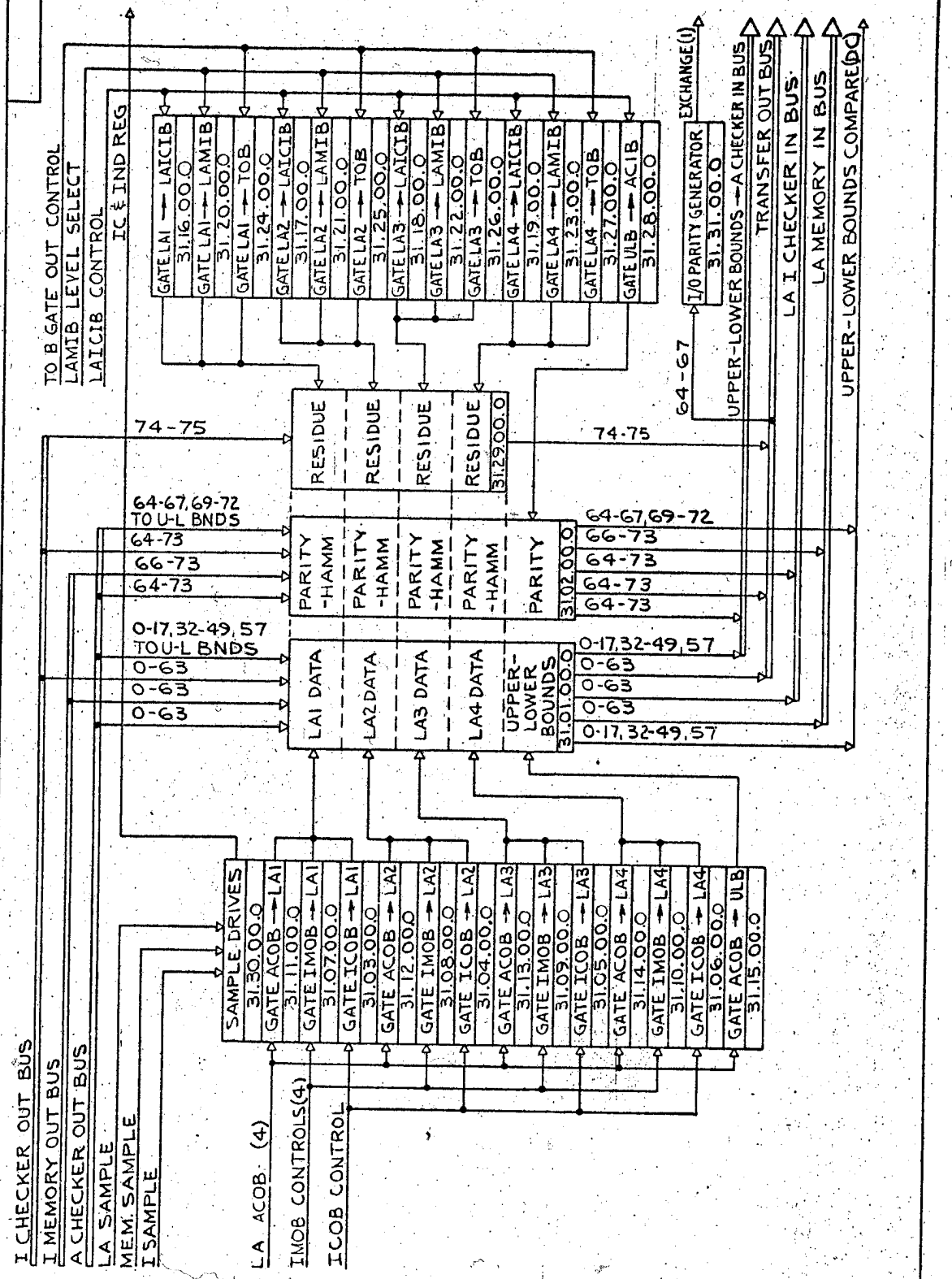

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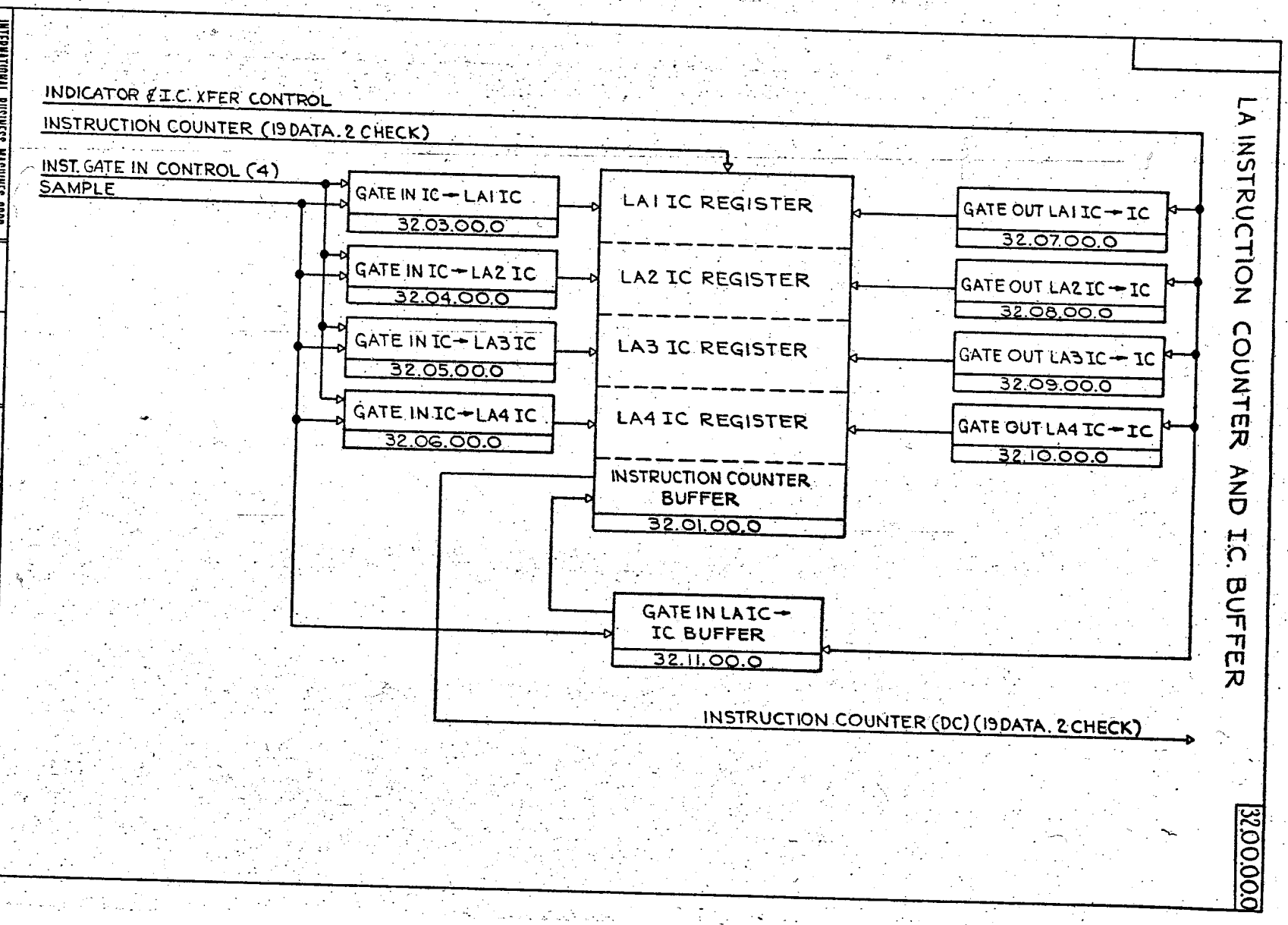
CHECK			DRAW						31.00.00.0
APPRO			CHECK						



INTERNATIONAL BUSINESS MACHINES CORP.

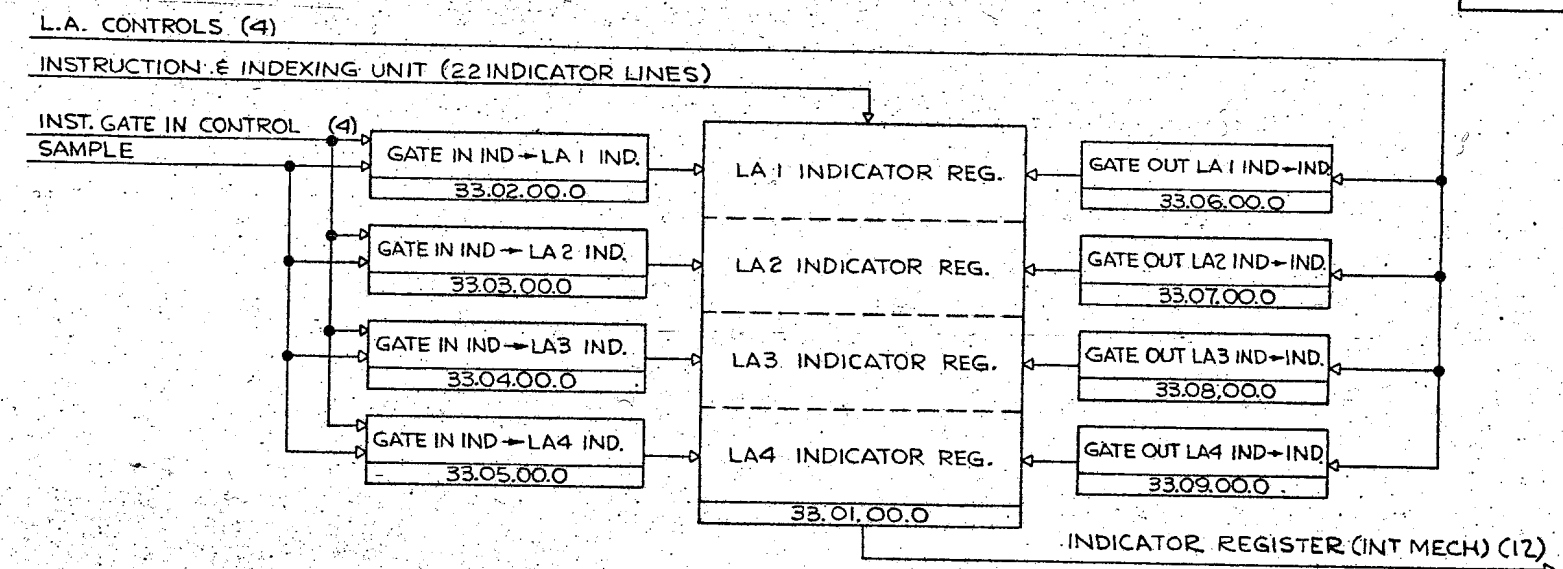
NAME	SYSTEMS DIAGRAM 32.00.00.0	DATE	—
DESIGN		CHANGE NO.	A
DETAIL	G.T. 1-19-59	DATE	/
CHECK		CHANGE NO.	
MODEL			
DRAW			
CHECK			
APPRO			

NOTE
X PRINT TO ENG. SPEC. NO.

DEVELOPMENT NO. 7000.20.1

32.00.00.0

19



L.A. INDICATOR REGISTERS

33.00.00.0

LOOKAHEAD INDICATORS

NO.	ABB.	NAME
0	CMK	CONDITIONAL MACHINE CHECK (2 GATES IN)
2	IR	INSTRUCTION REJECT (5 GATES IN)
15	OP	OPERATION CODE INVALID
16	AD	ADDRESS INVALID
19	DS	DATA STORE (2 GATES IN)
20	DF	DATA FETCH (2 GATES IN)
21	IF	INSTRUCTION FETCH
38	XF	INDEX FLAG
48	XCZ	INDEX COUNT ZERO
49	XVLZ	INDEX VALUE LESS THAN ZERO
50	XVZ	INDEX VALUE ZERO
51	XVGZ	INDEX VALUE GREATER THAN ZERO
52	XL	INDEX LOW
53	XE	INDEX EQUAL
54	XH	INDEX HIGH

INTERNATIONAL BUSINESS MACHINES CORP.

NAME: SYSTEMS DIAGRAM 33.00.00.0

DESIGN / DETAIL: GT 1-19-59 / CHECK / DRAW / CHECK / MODEL / APPRO

DATE: 3-2-59 — CHANGE NO.: A — DATE: ✓ — CHANGE NO.:

NOTE: X PRINT TO ENG. SPEC. NO.

DEVELOPMENT NO.: 7000.20.1

33.00.00.0

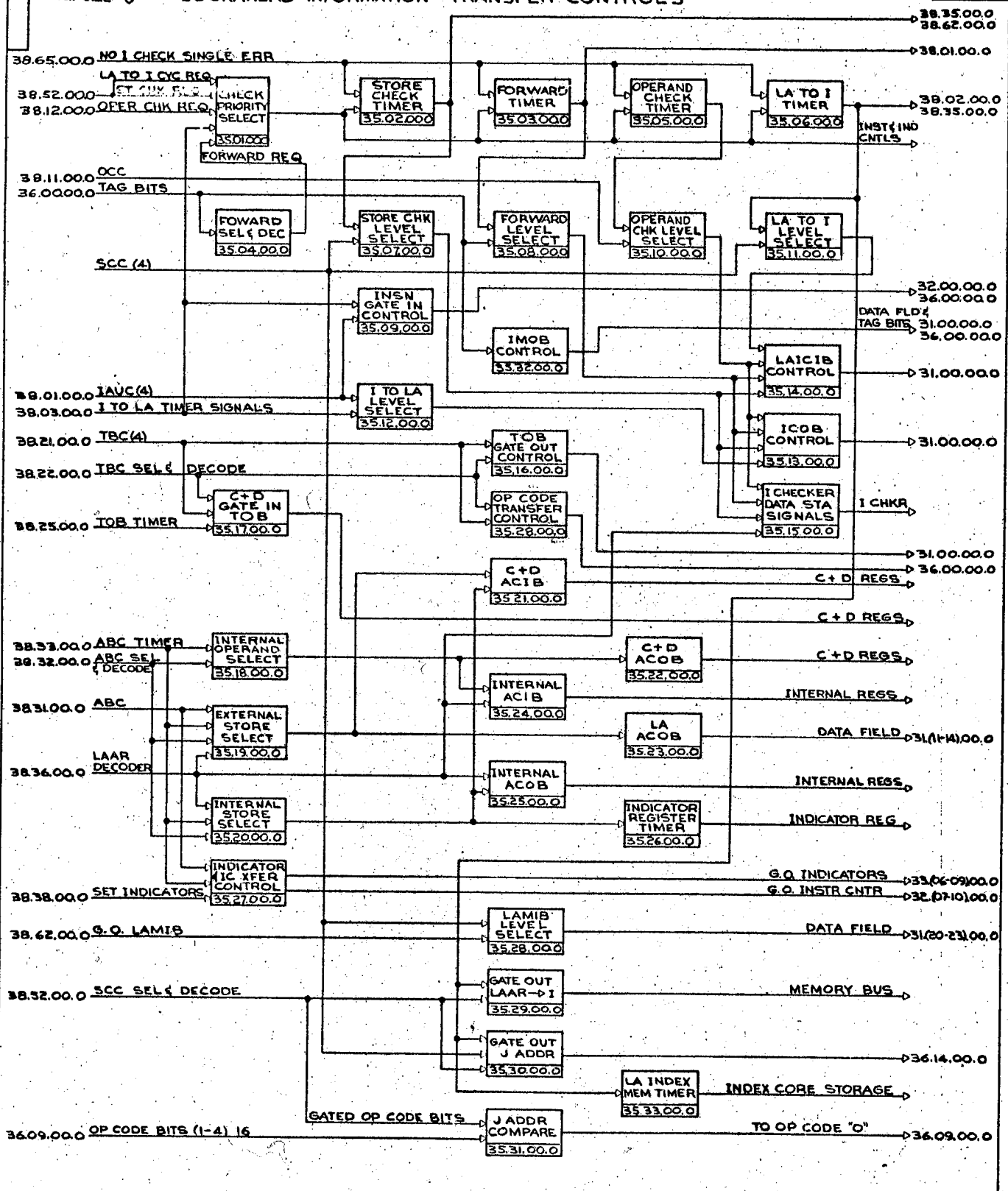
DEFIANCE NO. 88

FORM 96-6009-2

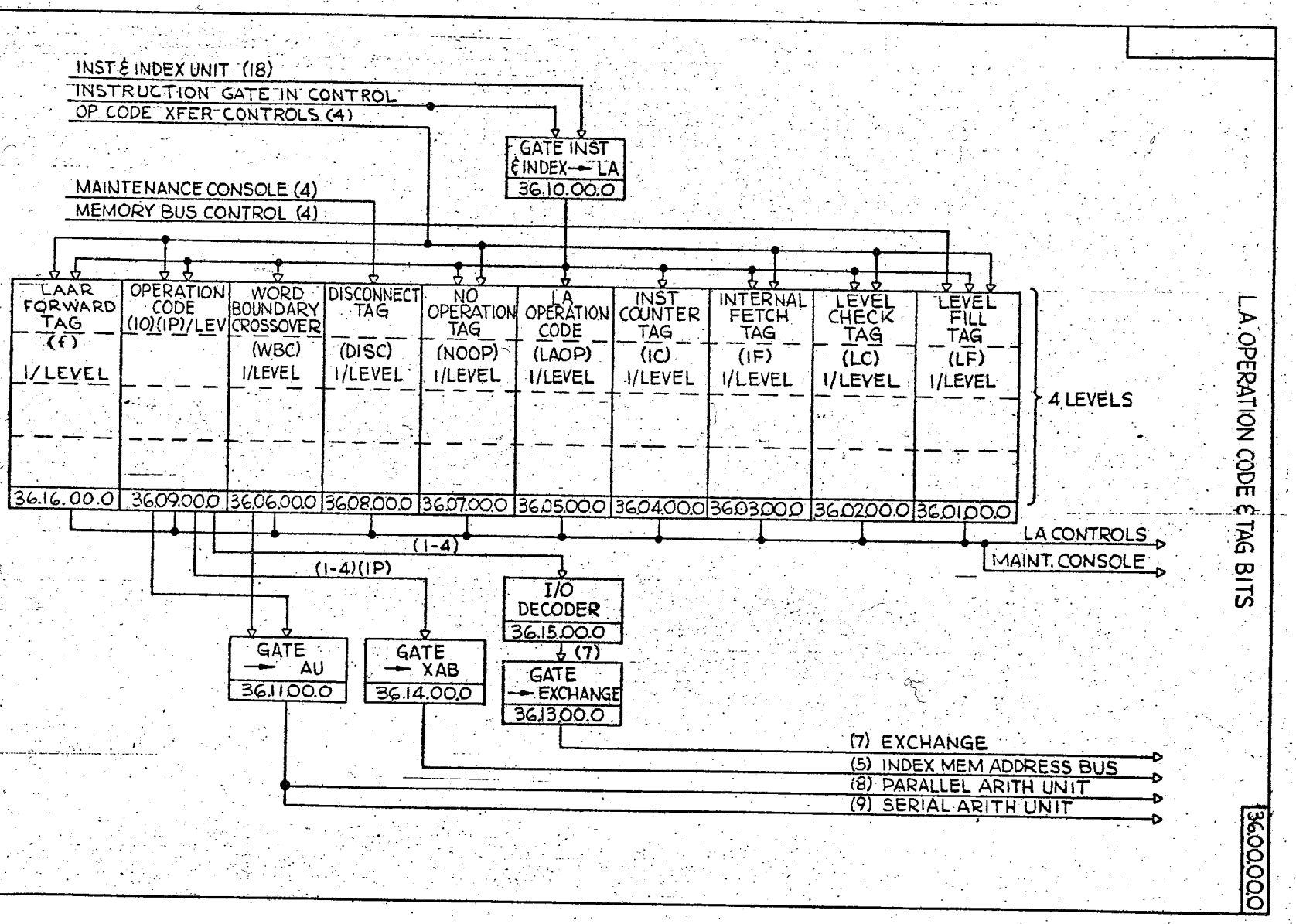
DWG. SIZE - C

LOOKAHEAD INFORMATION TRANSFER CONTROLS

35.00.00.0



INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME SYSTEMS DIAGRAM 35.00.00.0	—	A			X PRINT TO ENG. SPEC. NO.	
DESIGN / MODEL						
DETAIL G.T. 7-21-59						
CHECK / DRAW						35.00.00.0
APPRO / CHECK						



LA OPERATION CODE & TAG BITS

36.00.00.0

INTERNATIONAL BUSINESS MACHINES CORP.

NAME SYSTEMS DIAGRAM

36.00.00.0

DESIGN

DETAIL ID. 3359

MODEL

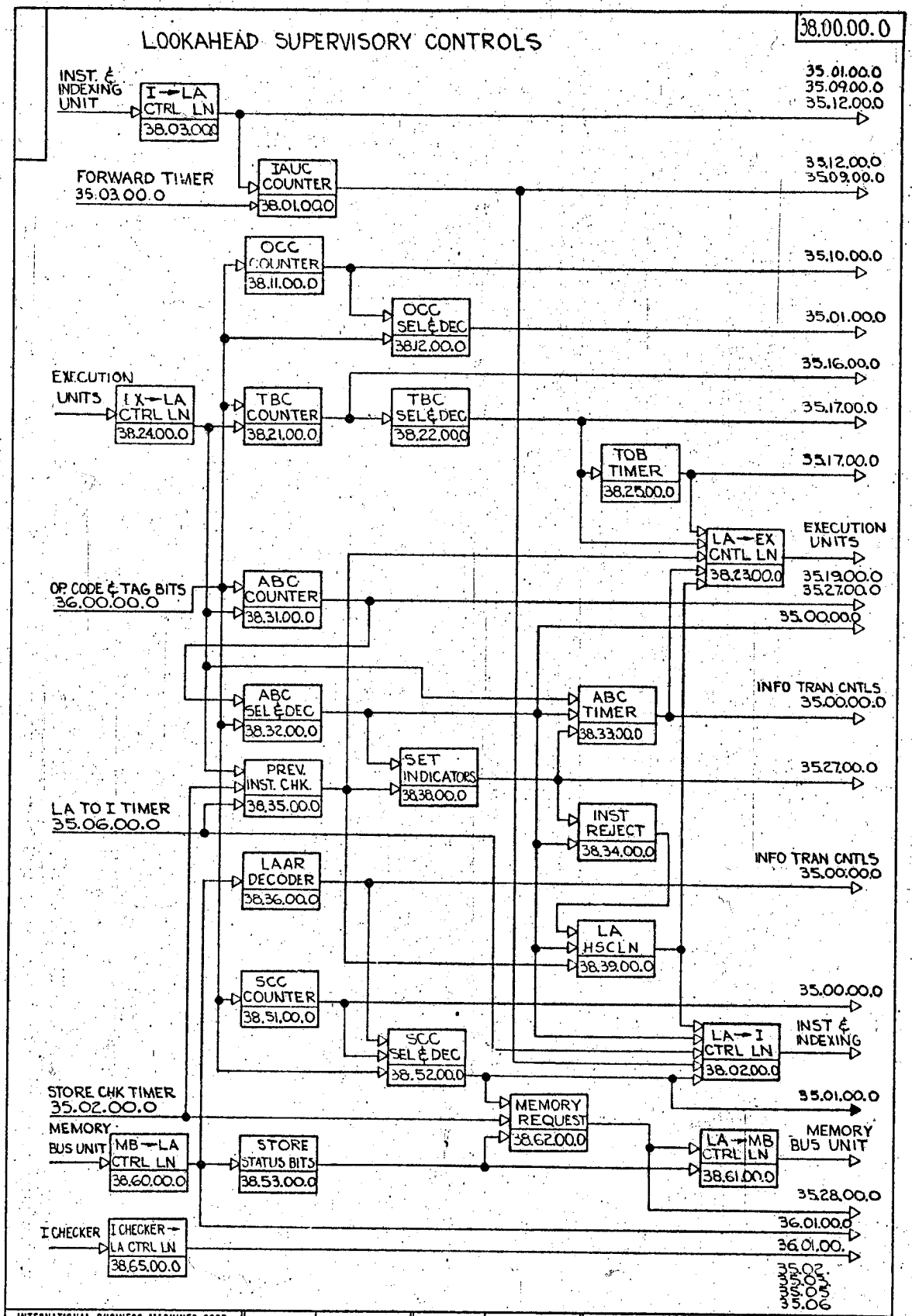
APPRO CHECK DRAW CHECK

DATE CHANGE NO. DATE CHANGE NO.

NOTE X PRINT TO ENG. SPEC. NO.

DEVELOPMENT NO. 36.00.00.0

DEFIANCE NO. 99



INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	DATE	CHANGE NO.	NOTE	DEVELOPMENT NO.
NAME	SYSTEMS DIAGRAM 38.00.00.0			—	A			X PRINT TO ENG. SPEC. NO.	
DESIGN	JD		MODEL	1-29-60	B				
DETAIL	JD	6-29-59							
CHECK			DRAW						38.00.00.0
APPRO			CHECK						

Appendix II

LOOKAHEAD LOADING LINE DEFINITION-CONTROL FUNCTIONS

	ANTIC IAUC ADV	SET LLP MEM	ANTIC I-II ENABLE	ANTIC III ENABLE	SET LAAR BUSY	RESET STORE EXEC	SET ABS FWD. REQ	SET FWD REQ.	RESET IAUC AES	DETERMINE CHKR PRIOR	NO. OF LINES (I BOX CONTROL AREA) LAL	E1	E2
COND IR-COND NOOP G1 PAR-TYPE I E.M	X	X	X	9							✓		
TYPE I E.M.	X	X	X	9								✓	✓
TYPE II E.M.		2	X	9		5	3	4			✓		✓
TYPE III E.M.	8	7	8		X	X					✓	✓	✓
LA LOAD EM̄									X		✓	✓	✓
CHECK CYCLE EM̄										X	✓	✓	✓
MPYC·LD·EM·TO·LA		INHIBIT GATE IN LAAR IF NO LAAR BUSY									✓		
TYPE II CANCEL MEM		REPLACE IAUC AES PARTICIPATION IN ENABLE SIGNALS									✓		
ECC CHECK LOAD		INHIBIT ACTION - SEE NOTES 7 & 8										✓	

2 W. MEM ACCEPT
3 IF COMPARE-IAUG$_i$-F$_i$
4 IF COMPARE
5 IF NO COMPARE. NO LAAR BUSY
7 IF NO SINGLE ECC ERR + NO "ECC-CHK-LD-E1"
8 IF NO "ECC-CHK-LD-E1"
9 IF NO LAAR BUSY

LOOKAHEAD LOADING LINE DEFINITION - INFORMATION TRANSFER

GATE IN OP CODE				GATE IN TAGBITS												GATE IN INDICATORS									GI IC FIELD	GATE IN OPERAND				NO OF LINES		
0-7	8		9 ECK	FROM		NO OP				WBC	LAOP	IC	INT	LC	LF	CNIDC	IR			DF		DS		OPAD-IF-UXIR	0-20	0-63	64-75	66-75		I BOX CONTROL AREA		
B	B	U	B	U	U	U	U	U	U	B	B	B	B	U	U	U	U	U		U	U	U	U	B	B	B	B	B	U = UNIPOLAR B = BIPOLAR CONTROL LINE	LAL	E_1	E_2
OP 0-7 BIT GI DIR	OP 8 BIT GI DIR	OP 8 BIT GI FR I PAR ERR	OP 9 ECK BITS GI DIR	FR BITS SET	FR BITS RES	NO OP BIT GI DIR	NO OP BIT GI FR I PAR ERR	NO OP BIT FR ECC ERR	NO OP BIT FR AL-ARM	WBC BIT GI DIR	LAOP BIT GI DIR	IC BIT GI DIR	INT BIT GI DIR	LC BIT SET	LF BIT SET	CNIBC BIT GI FR I PAR ERR	IR BIT GI DIR	IR BIT GI I PAR ERR		DF BIT GI DIR	DF BIT GI FR AL-ARM	DS BIT GI DIR	DS BIT GI FR AL-ARM	OP-AD-IF-UXIR BITS GI DIR	0-20 BITS GI DIR	0-20 BITS GI DATA	64-75 BITS GI PER	66-75 BITS GI ECC				
X	①		X		⑩	X	X			X	X	X	X	X	X		X	X		X		X		X	X	X			COND IR NOOP GI PAR TYPE I	✓		
X	①		X		⑩	X				X	X	X	X				X			X		X		X					TYPE I EM		✓	✓
X	①		X	⑤	⑤⑥	X				X	X	X	X				X			X		X		X					TYPE II EM	✓		✓
X	①		X	X	⑥	X				X	X	X	X	⑦	⑦		X			X		X		X	LAL ONLY				TYPE III EM	✓	✓	✓
																									LAL ONLY				COND IC FIELD		✓	✓
																									X							
																										X	X		DATA LD GATE DATA PAR		✓	✓
																										X		X	DATA LD GATE DATA ECC		✓	✓
																					X								COND LAD F FR ALARM	✓		✓
																							X						COND LAD S FR ALARM	✓	✓	✓
									X																				COND LA NOOP FR ALARM	✓	✓	✓
																		X											COND IR FR I PAR ERROR		✓	✓
							X																						COND CNI DC FR I PAR ERROR		✓	✓
																X													COND CNI DC FR I PAR ERROR		✓	✓
		X																											COND OP 8 FR I PAR ERROR		✓	✓
								X																		X	X		ECC CORRECT LOAD		✓	✓

① IF NO "COND OP 8 FR I PAR ERR"
⑤ IF NO COMPARE · NO LAAR BUSY
⑥ IF NO IAUC 2
⑦ IF NO SINGLE ECC ERR + NO "ECC · CHK · LD · E1"
⑩ IF NO IAUC 2

SPECIAL OPER AND FIELD FORMATS

	64	65	66	67	68	69	70	71	72	73
SAU INSTRUCTION OP CODE LEVEL	P 0 2 3 LENGTH 7	P 0-7 L 5 B BS 0-2 9-11 P 8-11 OFFSET 12 15	P 12-15 OFFSET 4-6 16 18 00000 19 23	P 16-23 00000000 24 31	P 24-31 00000000 1 32 39	P 32-39 00000000 1 40 47	P 40-47 00 1 48 49 BA 0-5 50 55	P 48-55 0000 56 59	P 54-59 0000 1 60 63	P 60-63 1
BRANCH ON BIT OP CODE LEVEL	00000000 0 7	P 0-7 1 0000 8 11 P 8-11 1 0000 12 15	P 12-15 1 00000000 16 23	P 16-23 1 00000000 24 31	P 24-31 1 00000000 32 39	P 32-39 1 00000000 40 47	P 40-47 1 00 48 49 BA 0-5 50 55	P 48-55 0000 56 59	P 54-59 1 LLF IZN I 60 63	P 60-63
BRANCH ON INDICATOR OP CODE LEVEL	00000000 0 7	P 0-7 1 0000 8 11 P 8-11 1 0000 12 15	P 12-15 1 00000000 16 23	P 16-23 1 00000000 24 31	P 24-31 1 00000000 32 39	P 32-39 1 00000000 40 47	P 40-47 1 00 48 49 IA 0-5 50 55	P 48-55 0000 56 59	P 54-59 1 0 LF ZN I 60 63	P 60-63
PSEUDO BR ON IND FOR IRPT OP CODE LEVEL	RANDOM 0 7	P 0-7 RANDOM 8 11 P 8-11 IND ADDR 0-5 12 15	P 12-15 IA 4-5 16 17 RANDOM 18 23	P 16-23 00000000 24 31	P 24-31 1 00000000 32 39	P 32-39 1 00000000 40 47	P 40-47 1 00000000 48 55	P 48-55 1 0000 56 59	P 54-59 1 0 LF ZN I 60 63	P 60-63
BRANCH RECOVERY LEVEL	BR ADDR 0-7 0 7	P 0-7 BR ADDR 8-11 8 11 P 8-11 BR ADDR 12-15 12 15	P 12-15 BR ADDR 16- 18 0000 19 23	P 16-23 00000000 24 31	P 24-31 1 00000000 32 39	P 32-39 1 00000000 40 47	P 40-47 1 00000000 48 55	P 48-55 1 0000 56 59	P 54-59 1 0000 60 63	P 60-63 1
SAU IMM DATA	DATA 0-7 0 7	P 0-7 DATA 8-11 8 11 P 8-11 DATA 12-15 12 15	P 12-15 DATA 16-23 16 23	P 16-23 D 24 24 00000000 25 31	P 24-31 00000000 32 39	P 32-39 00000000 40 47	P 40-47 1 00000000 48 55	P 48-55 1 0000 56 59	P 54-59 1 0000 60 63	P 60-63 1
PAU IMM DATA	DATA 0-7 0 7	P 0-7 DATA 8-11 8 11 P 8-11 RANDOM 12 15	P 12-15 RANDOM 16 23	P 16-23 00000000 24 31	P 24-31 1 00000000 32 39	P 32-39 1 00000000 40 47	P 40-47 1 00000000 48 55	P 48-55 1 0000 56 59	P 54-59 1 0000 60 63	P 60-63 1
INPUT OUTPUT	CWA 0-7 0 7	P 0-7 CWA 8-11 8 11 P 8-11 CWA 12-15 12 15	P 12-15 CWA 16-17 16 17 00000 18 23	P 16-23 00000000 24 31	P 24-31 1 CHAN ADDR 0-6 32 38 0 39	P 32-39 00000000 40 47	P 40-47 1 00000000 48 55	P 48-55 1 0000 56 59	P 54-59 1 0000 60 63	P 60-63 1

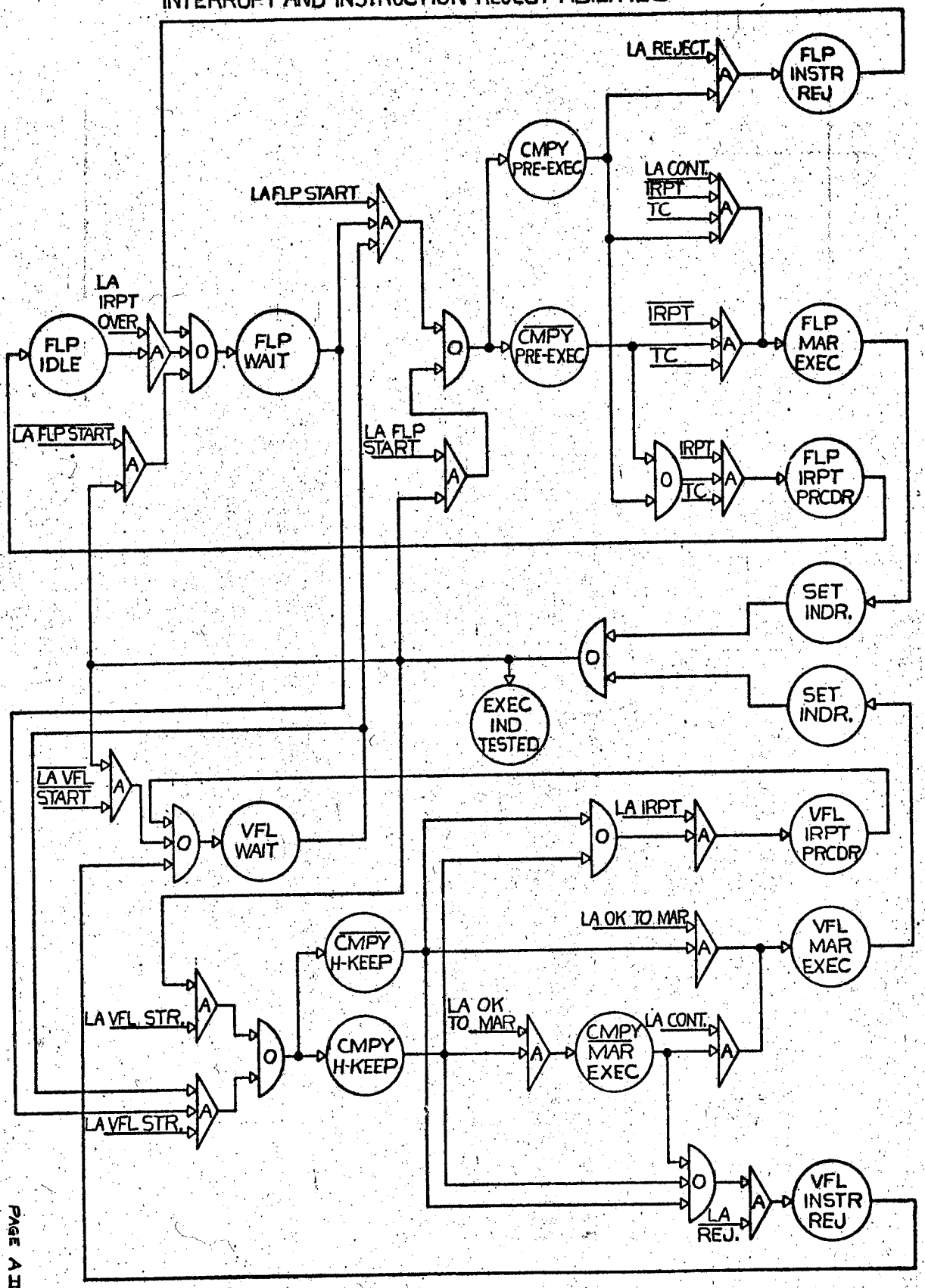
LEVEL | AA | 10-27-59 | WCS

LOOKAHEAD OPERATION CODE FIELD FORMATS

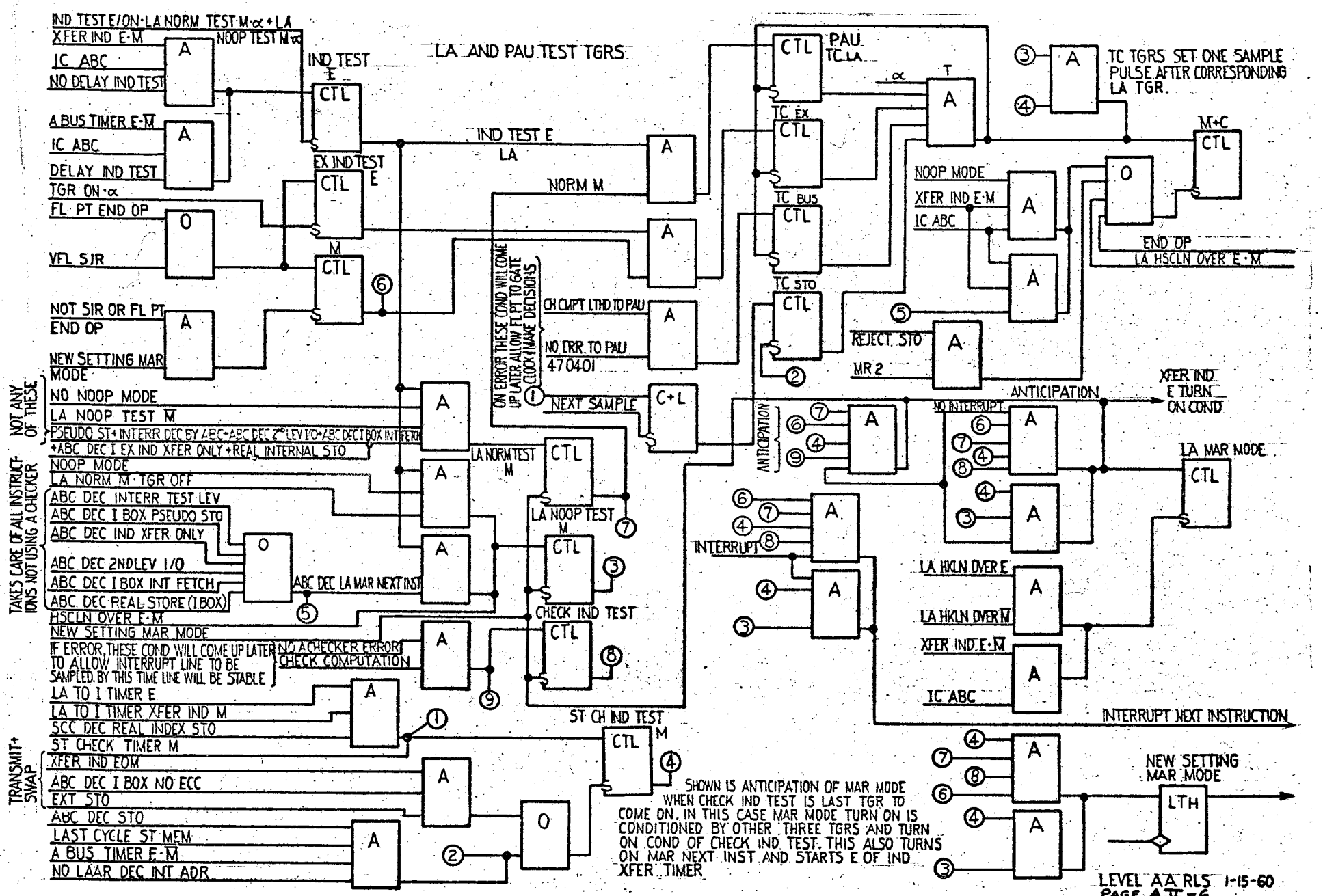
	0	1	2	3	4	5	6	7	8	9	P	LAOP TAG BIT
CONNECT		C	C	C	C	OP CODE						
SAU INSTRUCTION Op CODE LEVEL INTEGER	OFF 7	SIGN		BIN/DEC	OPERATION CODE					1	0-9	0
BRANCH ON INDICATOR/ BIT Op CODE LEVEL	LAOP$_0$	CONDITIONAL INDICATORS AD	EXE	DS	IF	LAOP$_{5-9}$					RANDOM	1
PAU INSTRUCTION	N/U	SIGN		OPERATION CODE					1	0	0-9	0
INPUT / OUTPUT Op CODE LEVEL	RANDOM	OPERATION CODE				1	0	BX=0 HSX=1	0	0	RANDOM	0
PSEUDO STORE LEVEL	LAOP$_0$	XCS ADDR				LAOP$_{5-9}$					1-4	1
ALL OTHER LEVELS	LAOP$_0$	RANDOM				LAOP$_{5-9}$					RANDOM	1

LEVEL	AB	1-20-60	WCS

EXECUTION UNIT STATES REQUIRED FOR PROGRAM INTERRUPT AND INSTRUCTION REJECT ABILITIES

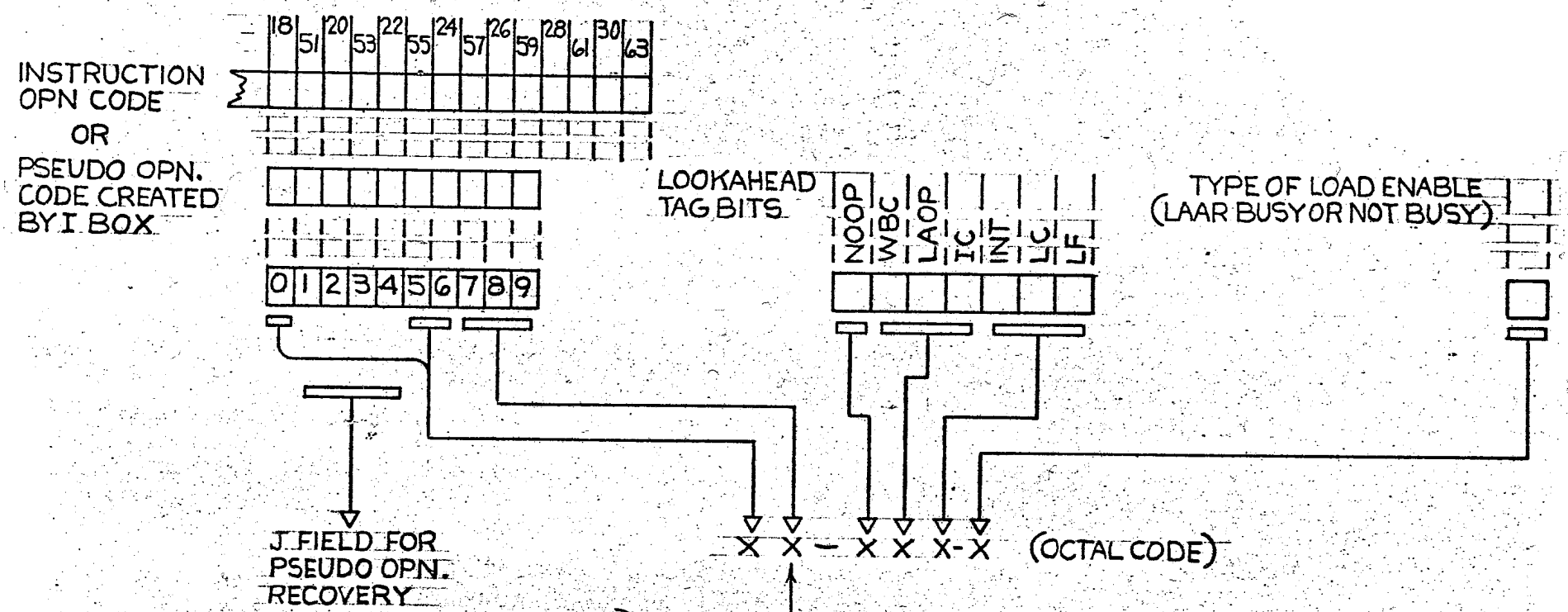


LEVEL | AA | 10-27-59 | WCS


LA AND PAU TEST TGRS
IND TEST E/ON·LA NORM TEST·M·α+LA
XFER IND E·M
IC ABC
NO DELAY IND TEST
NOOP TEST M·α
A BUS TIMER E·M
IC ABC
DELAY IND TEST
TGR ON·α
FL PT END OP
VFL SJR
NOT SIR OR FL PT
END OP
NEW SETTING MAR MODE
IND TEST E
EX IND TEST E
M
IND TEST E LA
NORM M
ON ERROR THESE COND WILL COME UP LATER ALLOW FL PT TO GATE CLOCK & MAKE DECISIONS
CH CMPT LTH TO PAU
NO ERR TO PAU
470401
NEXT SAMPLE
PAU TC LA
TC EX
TC BUS
TC STO
REJECT STO
MR 2
TC TGRS SET ONE SAMPLE PULSE AFTER CORRESPONDING LA TGR.
M+C
NOOP MODE
XFER IND E·M
IC ABC
END OP
LA HSCLN OVER E·M
NOT ANY OF THESE
NO NOOP MODE
LA NOOP TEST M
PSEUDO ST+INTERR DEC BY ABC+ABC DEC 2ND LEV IO+ABC DEC I BOX INT FETCH
+ABC DEC I EX IND XFER ONLY+REAL INTERNAL STO
TAKES CARE OF ALL INSTRUCTIONS NOT USING A CHECKER
NOOP MODE
LA NORM M·TGR OFF
ABC DEC INTERR TEST LEV
ABC DEC I BOX PSEUDO STO
ABC DEC IND XFER ONLY
ABC DEC 2ND LEV I/O
ABC DEC I BOX INT FETCH
ABC DEC REAL STORE (I BOX)
ABC DEC LA MAR NEXT INST
HSCLN OVER E·M
NEW SETTING MAR MODE
IF ERROR, THESE COND WILL COME UP LATER TO ALLOW INTERRUPT LINE TO BE SAMPLED. BY THIS TIME LINE WILL BE STABLE
NO A CHECKER ERROR
CHECK COMPUTATION
LA NORM TEST M
LA NOOP TEST M
CHECK IND TEST
ANTICIPATION
INTERRUPT
NO INTERRUPT
XFER IND E TURN ON COND
LA MAR MODE
LA HKLN OVER E
LA HKLN OVER M
XFER IND E·M
IC ABC
INTERRUPT NEXT INSTRUCTION
TRANSMIT+SWAP
LA TO I TIMER E
LA TO I TIMER XFER IND M
SCC DEC REAL INDEX STO
ST CHECK TIMER M
XFER IND EOM
ABC DEC I BOX NO ECC
EXT STO
ABC DEC STO
LAST CYCLE ST MEM
A BUS TIMER E·M
NO LAAR DEC INT ADR
ST CH IND TEST M
SHOWN IS ANTICIPATION OF MAR MODE WHEN CHECK IND TEST IS LAST TGR TO COME ON. IN THIS CASE MAR MODE TURN ON IS CONDITIONED BY OTHER THREE TGRS AND TURN ON COND OF CHECK IND TEST. THIS ALSO TURNS ON MAR NEXT INST AND STARTS E OF IND XFER TIMER
NEW SETTING MAR MODE
LTH

Appendix III

LOOKAHEAD UNIT
DEFINITION OF LEVEL DESIGNATION FOR LOADING SEQUENCE



This octal digit, when designated as a 1 for the 1st level of SAU instructions implies only the presence of Op Code bit 9, since Op Code bits 7 & 8 are defined only by the particular SAU operation code buffered in this level.

This octal digit, when designated as a 2 for the 1st level of PAU instructions implies only the presence of Op Code bit 8 and absence of Op Code bit 9, since Op Code bit 7 is defined only by the particular PAU operation code buffered at this level.

NOOP — NO OPERATION BIT
WBC — WORD BOUNDARY CROSS OVER
LAOP — LOOKAHEAD OPERATION CODE
IC — INSTRUCTION COUNTER BIT
INT — INTERNAL OPERAND BIT
LC — LEVEL CHECKED BIT
LF — LEVEL FILLED OUT
PX — PROGRESSIVE INDEXING

LOOK AHEAD

F. P. LOADING SEQUENCES

18 20 22 24 26 51 53	55	57 59	MNEMONIC	Supervisory Control WBC	PX	OP1	OP2	L. A. Loading Types 1st Level	2nd Level	3rd Level	4th Level	5th Level	6th Level	
VVV 0	000	010	/	NO	NO	EXT		2-010-1						I Non Store Operations
0	000	110	L			XS		2-013-1						
						INT		2-017-3						
0	010	010	K											
0	010	110	KR											
0	011	010	*											
0	011	110	/											
0	100	010	AU											
0	100	110	LWF											
0	110	010	KF											
0	110	110	KFR											
0	111	110	R/											
1	000	010	D /											
1	000	110	DL											
1	010	010	F /											
1	010	110	E /											
1	011	010	D *											
1	100	010	DAU											
1	100	110	DLWF											
1	110	010	SHF											
1	110	110	E / AI											
0	001	010	M /	NO	NO	EXT		2-000-1	13-033-3					II Add to Mem OPNS
						XS		2-003-1	"					
0	101	010	AUM			INT		2-007-3	"					
1	001	010	LFT	NO	NO	EXT		2-000-1	13-033-3					III Load Factor (Cum. M'cand)
						XS		2-003-1	"					
1	011	110	D/			INT		2-007-3	"					
0	111	010	* /	NO	No	EXT		2-000-1	11-030-1					IV Cumulative Multiply
						XS		2-003-1	"					
						INT		2-007-3	"					
0	001	110	ST	NO	NO	EXT		2-013-3						V Store Operations
						XS		"						
0	101	110	SRD			INT		"						
1	001	110	SLO											
1	101	110	SRT											

VFL LOADING SEQUENCES

18 20 22 24 26 51 53	55	57 59	MNEMONIC	Supervisory Control WBC	PX	OP1	OP2	L. A. Loading Types 1st Level	2nd Level	3rd Level	4th Level	5th Level	6th Level	
VVV	000	001	/	NO	NO	EXT		1-003-1	05-030-1					*04-033-1 Becomes 06-033-1 If no-op Code.
	000	011	LCV			XS		"	05-033-1					
	000	101	L			INT		"	05-037-3					
.....	00	111	C											
				NO	Yes	EXT		1-003-1	05-020-1	04-033-1*				I - No Store Opn Possible
	010	001	K			XS		"	05-023-1	"				
	010	011	KE			INT		"	05-027-3	"				
.....	10	111	CT	Yes	No	EXT	EXT	1-043-1	03-020-1	07-030-1				
0	011	001	*			EXT	XS	"	"	07-033-1				
	011	011	CV			EXT	INT	"	"	07-037-3				
	100	001	AU			XS	EXT	"	03-023-1	07-030-1				
						XS	XS	"	"	07-033-1				
	100	101	LWF			XS	INT	"	"	07-037-3				
						INT	EXT	"	03-027-3	07-030-1				
	110	001	KF			INT	XS	"	"	07-033-1				
	110	011	KFE			INT	INT	"	"	07-037-3				
	110	101	KFR											
	110	111	CT	Yes	Yes	EXT	EXT	1-043-1	03-020-1	07-020-1	04-033-1*			
						EXT	XS	"	"	07-023-1	"			
	111	011	DCV			EXT	INT	"	"	07-027-3	"			
						XS	EXT	"	03-023-1	07-020-1	"			
						XS	XS	"	"	07-023-1	"			
						XS	INT	"	"	07-027-3	"			
						INT	EXT	"	03-027-3	07-020-1	"			
						INT	XS	"	"	07-023-1	"			
						INT	INT	"	"	07-027-3	"			
	001	001	M /	No	No	EXT		1-003-1	05-020-1	17-033-3				II Possible to have two store functions.
						XS		"	05-023-1	"				
	001	101	ST			INT		"	05-027-3	"				
	001	111	CM											
				No	Yes	EXT		1-003-1	05-020-1	17-023-3	04-033-1*			
	101	001	AUM			XS		"	05-023-1	"	"			
	101	011	M / 1			INT		"	05-023-3	"	"			
	101	101	SRND											
	101	111	CM	Yes	No	EXT	EXT	1-043-1	03-020-1	07-020-1	17-023-3	23-033-3		
						EXT	XS	"	"	07-023-1	"	"		
						EXT	INT	"	"	07-027-3	"	"		
						XS	EXT	"	03-023-1	07-020-1	"	"		
						XS	XS	"	"	07-023-1	"	"		
						XS	INT	"	"	07-027-3	"	"		
						INT	EXT	"	03-027-3	07-020-1	"	"		
						INT	XS	"	"	07-023-1	"	"		
						INT	INT	"	"	07-027-3	"	"		

VFL LOADING SEQUENCES

18 20 22 24 26	51 53	55	57 59	MNEMONIC	Supervisory Control WBC	PX	OP1	OP2	L. A. Loading Types 1st Level	2nd Level	3rd Level	4th Level	5th Level	6th Level	
					Yes	Yes	EXT	EXT	1-043-1	03-020-1	07-030-1	17-023-3	23-023-3	04-033-1*	
							EXT	XS	"	"	07-023-1	"	"	"	
							EXT	INT	"	"	07-027-3	"	"	"	
							XS	EXT	"	03-023-1	07-020-1	"	"	"	
							XS	XS	"	"	07-023-1	"	"	"	
							XS	INT	"	"	07-027-3	"	"	"	
							INT	EXT	"	03-027-3	07-020-1	"	"	"	
							INT	XS	"	"	07-023-1	"	"	"	
							INT	INT	"	"	07-027-3	"	"	"	
	VVV	001	011	LFT	No	No	EXT		1-003-1	05-020-1	21-033-3				*04-033-1 Becomes 06-033-1 If No-op Code
							XS		"	05-023-1	"				
	1	011	001	* (Dec)			INT		"	05-027-3	"				
	1	011	101	/ (Dec)	No	Yes	EXT		1-003-1	05-020-1	21-023-3	04-033-1*			III Possible to have two fetch opns but only one store opn.
							XS		"	05-023-1	"	"			
		100	011	LTRCV			INT		"	05-027-3	"	"			
	1	111	001	* / (Dec)	Yes	No	EXT	EXT	1-043-1	03-020-1	07-020-1	21-033-3			
							EXT	XS	"	"	07-023-1	"			
		111	101	LTRS			EXT	INT	"	"	07-027-3	"			
						XS	XS	EXT	"	03-023-1	07-020-1	"			
							XS	XS	"	"	07-023-1	"			
							INT	EXT	"	03-027-3	07-020-1	"			
							INT	XS	"	"	07-023-1	"			
							INT	INT	"	"	07-027-3	"			
					Yes	Yes	EXT	EXT	1-043-1	03-020-1	07-020-1	21-023-3	04-033-1*		
							EXT	XS	"	"	07-023-1	"	"		
							EXT	INT	"	"	07-027-3	"	"		
							XS	EXT	"	03-023-1	07-020-1	"	"		
							XS	XS	"	"	07-023-1	"	"		
							XS	INT	"	"	07-027-3	"	"		
							INT	EXT	"	03-027-3	07-020-1	"	"		
							INT	XS	"	"	07-023-1	"	"		
							INT	INT	"	"	07-027-3	"	"		
	0	111	001	* / (bin)	No	No	EXT		1-003-1	05-020-1	15-030-1				
							XS		"	05-023-1	"				
							INT		"	05-027-3	"				
					No	Yes	EXT		1-003-1	05-020-1	15-020-1	04-033-1*			
							XS		"	05-023-1	"	"			
							INT		"	05-027-3	"	"			
					Yes	No	EXT	EXT	1-043-1	03-020-1	07-020-1	15-030-1			
							EXT	XS	"	"	07-023-1	"			
							EXT	INT	"	"	07-027-3	"			
							XS	EXT	"	03-023-1	07-020-1	"			
							XS	XS	"	"	07-023-1	"			
							XS	INT	"	"	07-027-3	"			

VFL LOADING SEQUENCES

18 20 22 24 26	51 53	55	57 59	MNEMONIC	Supervisory Control WBC	PX	OP1	OP2	L. A. Loading Types 1st Level	2nd Level	3rd Level	4th Level	5th Level	6th Level	
							INT	EXT	1-043-1	03-027-3	07-020-1	15-030-1			
							INT	XS	"	"	07-023-1	"			
							INT	INT	"	"	07-027-3	"			
					Yes	Yes	EXT	EXT	1-043-1	03-020-1	07-020-1	15-020-1	04-033-1*		
							EXT	XS	"	"	07-023-1	"	"		
							EXT	INT	"	"	07-027-3	"	"		
							XS	EXT	"	03-023-1	07-020-1	"	"		
							XS	XS	"	"	07-023-1	"	"		
							XS	INT	"	"	07-027-3	"	"		
							INT	EXT	"	03-027-3	07-020-1	"	"		
							INT	XS	"	"	07-023-1	"	"		
							INT	INT	"	"	07-027-3	"	"		
			100	BI	No	No	INT		35-023-1 SEE NOTE 1	37-027-3	41-023-1	45-033-1 SEE NOTE 2			V Branch Indicator 1. If intrpt-Bin Level use 75-023-1 2. 45-033-1 becomes 47-033-1 if nnop code
			100	SICBI	No	No	INT	EXT	35-023-1	37-027-3	41-023-1	45-023-1	31-073-3 (57-033-1)		BR Successful cond ind, level 5 as shown. Br. successful cond ind, level 5 becomes 57-033-1 since no "SIC"
							INT	XS	"	"	"	"			
							INT	INT	"	"	"	"			
	111	000	000	BB	No	No	EXT		43-023-1	05-020-1	17-023-3	45-033-1			
							XS		"	05-023-1	"	"			
							INT		"	05-027-3	"	" SEE NOTE 2			
									INPUT - OUTPUT LOADING SEQUENCES						
	100	010	000	CCW					20-003-1	65-003-1					
	000	010	000	RD					20-003-1	25-033-1					
	000	110	000	W											
	001	010	000	CTL											
BX	001	110	000	LOC											
	010	110	000	WE											
	011	010	000	CTLE											
	011	110	000	LOCE											
	100	110	000	REL											
	110	110	000	RELE											
	100	010	000	CCW					24-003-1	65-033-1					
HX				CCW					24-003-1	25-033-1					
	Pseudo Store			PX 1, 2, 5, 6					04-033						LOP 1
	Pseudo Store			PX 3, 7					04-033						LOP 2
	No Oped			PX 1, 2, 5, 6					06-033						LOP 1
	No Oped			PX 3, 7					06-033						LOP 2

LOOK AHEAD.

I BOX LOADING SEQUENCES

	Name	MNEMONIC	FORM DIR	FORM IMM	OPND SRCE EXT	OPND SRCE XS	OPND SRCE INT	L. A. LOADING TYPES 1st Level	2nd Level	3rd Level	4th Level	Cycle
I	CZRF - M	V / ICR		X								LOP 2
	Load Index	LX	X		X	X		02-1/0 33-1	(Pseudo Store)			LOP 1
	Load Value	LV	X		X	X						LOP 1
	Load Count	LC	X		X	X						LOP 1
	Load Refill	LR	X		X	X						LOP 1
	Store Index	SX	X			X						LOP 1
	Store Value	SV	X			X						LOP 1
	Store Count	SC	X			X						LOP 1
	Store Refill	SR	X			X						LOP 1
	Increment	V /	X		X	X						LOP 1
	Incr. & Cnt.	V / C	X		X	X						LOP 1
	Incr. Cnt. & Ref. (NM)	V / CR	X		X	X						LOP 1
	Compare Value	KV	X		X	X						LOP 1
	Compare Count	KC	X		X	X						LOP 1
	Load Value IMM	LVI		X								LOP 1
	Load Count IMM	LCI		X								LOP 1
	Load Refill IMM	LRI		X								LOP 1
	Increment IMM	V / I		X								LOP 1
	Incr. Neg. IMM	V - I		X								LOP 1
	Incr. & Cnt. IMM	V / IC		X								LOP 1
	Incr. Neg. & Cnt. IMM	V - IC		X								LOP 1
	Incr. Cnt. & Ref. IMM (NM)	V / ICR		X								LOP 1
	Incr. Neg. Cnt. & Ref. (NM)	V - ICR		X								LOP 1
	Add to Count IMM	C / I		X								LOP 1
	Add Neg. to Cnt. IMM	C - I		X								LOP 1
	Refill ZRO Cnt (Cnt-O)	RCZ	X			X						LOP 2
	Refill ZRO Cnt (Cnt-O)	RCZ	X		X	X						LOP 1
	Refill	R	X		X	X						LOP 1
	Store Valin Addr	SVA	X			X						LOP 1
	Store Zero	Z	X			X						LOP 1
	LD Val. Effect	LVE	X		X	X						LOP 1
	LD Val Wi Sum	LVS		X								LOP 1
	Comp Valve IMM	KVI		X								LOP 1
	Comp Val. Neg. IMM	KVNI		X								LOP 1
	Comp. Cnt. IMM	KCI		X								LOP 1
	Load Val. Neg. IMM	LVNI		X								LOP 1
	CZRF - M	V / CR	X		X	X						LOP 2
II		SX	X		X			33-1/073-3	(Real Ext Store in ECC)			LST 1
		SV	X		X							LST 1
		SC	X		X							LST 1
		SR	X		X							LST 1
		R	X		X							LST 1
	Ref. Cnt Zro, Cnt - O	RCZ	X		X							LST 1
		SVA	X		X							LST 1
		Z	X		X							LST 1
III		SX	X				X	33-1/0 33-3	(Real Store in P & R)			LST 1
		Z	X				X					LST 1
IV		SV	X				X	51-027-3	33-1/0 33-3			IRF 1
		SC	X				X	(int. fetch				LST 1
		SR	X				X	request)				LST 1
		R	X				X					LST 1
	Cnt - O	RCZ	X				X					LST 1
		SVA	X				X					LST 1
V		LX	X				X	51-027-3	02-1/0 33-1			IRF 1
		LV	X				X					LOP 1
		LC	X				X					LOP 1
		LR	X				X					LOP 1
		V /	X				X					LOP 1
		V / C	X				X					LOP 1
	CZRF - NM	V / CR	X				X					LOP 1
		LVE	X				X	(May be more than one IRF Level)				LOP 1
		KV	X				X					LOP 1
		KC	X				X					LOP 1
	CZRF - M	V / CR	X				X					IRF 1, LOP 2
VI	RZC C-O				X	X		63-1/0 33	(Ind Transfer only)			LOP 1
	RZC C-O						X	51-029	63-1/0 33-1			IRF 2, LOP 1
								(Int fetch- Ind Xfer)				

LOOK AHEAD

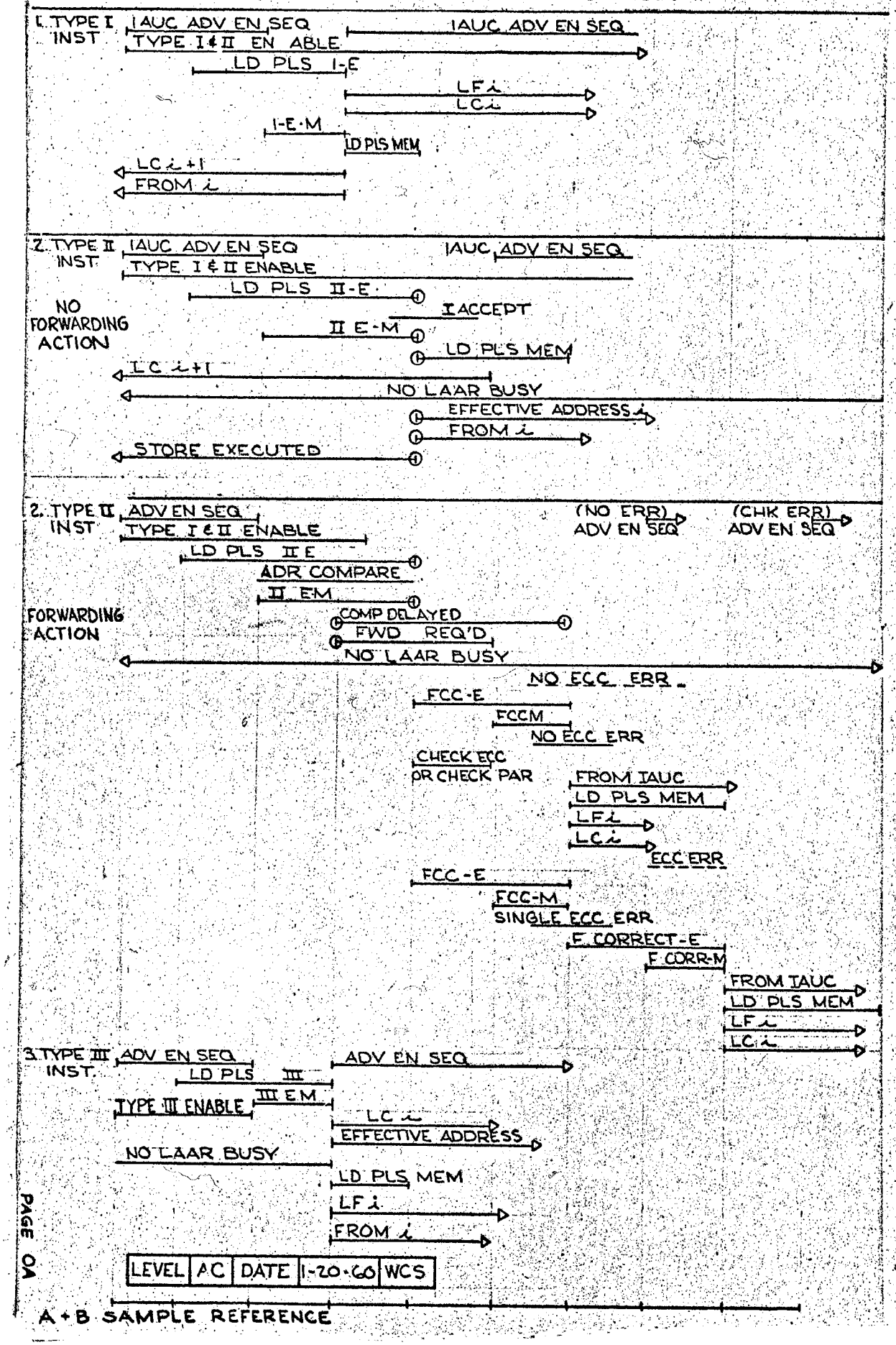
I BOX LOADING SEQUENCES

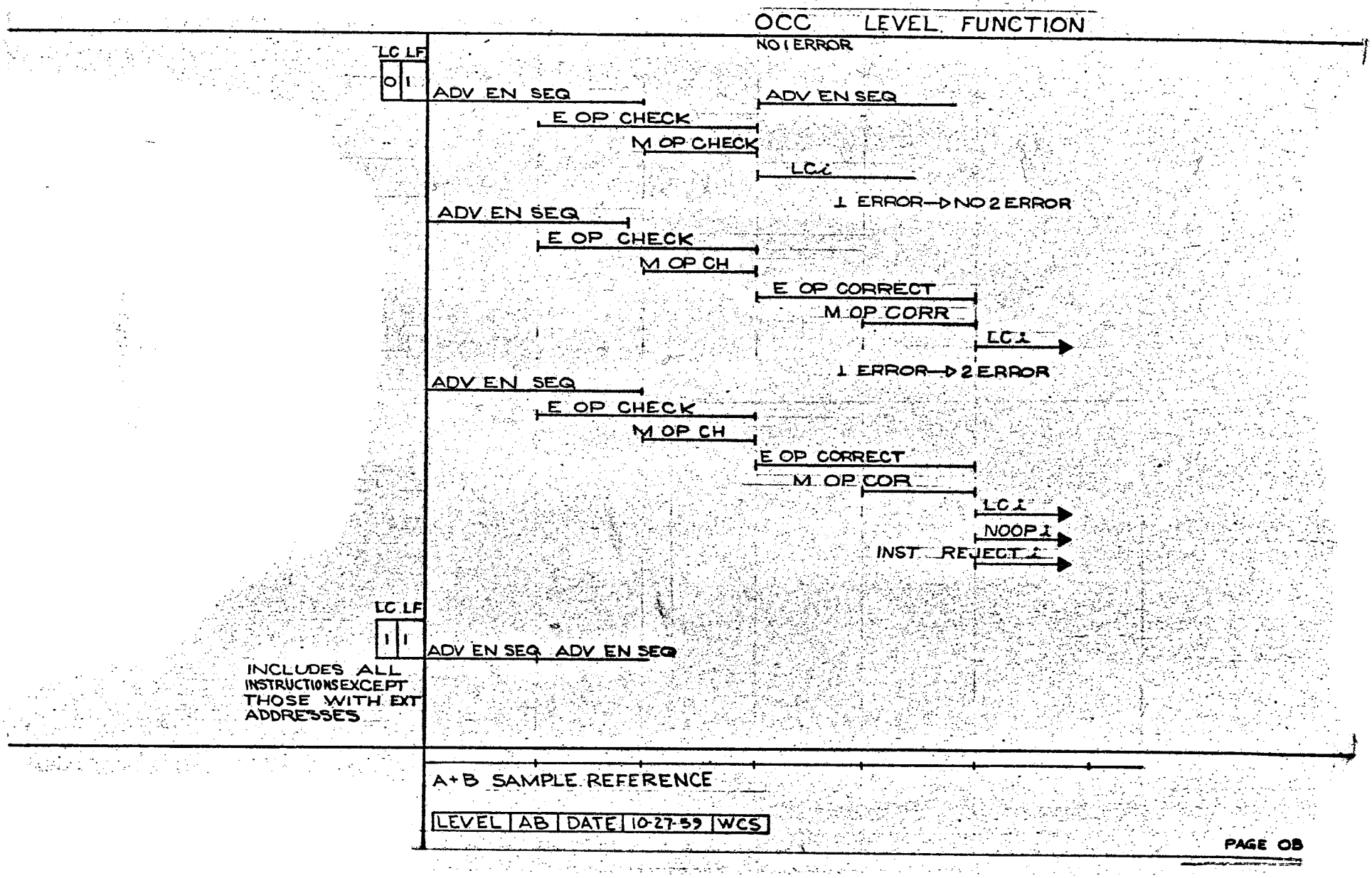
	Name	MNEMONIC	FORM DIR	FORM IMM	OPND SRCE EXT	OPND SRCE XS	OPND SRCE INT	L. A. LOADING TYPES 1st Level	2nd Level	3rd Level	4th Level	Cycle
VII	Rename	RNX	X					00-023-1				AOO 1
	Rename If Intrpt or Nop	RNX	X					" (clear LA level)	02-033-1 (pseudo store)			LOP 1
	Rename Normal	RNX	X					"	33-063-3	63-033-1		
	Rename Normal	RNX	X					"	" Real Ext. Store	Ind Xfer Only		
VIII	Transmit-Swap	T Swap			X			00-023-1 (test level)	33-063-3 or 33-023-3 (Ext Store or Int Str)	63-033-3 (Ind. Xfer only)		ADD 1 IRF 3 IRF 4 LST 3 LOP 1
							X	00-023-1	51-027-3 (I Bx Int Fetch)	33-033-3		
IX	Execute Indirect If No Opd	EXIC						33-063-3 Sp Ext Store 33-173-3 Real Ext St	Any other Instruction Level			
	BRANCH INSTRUCTIONS											
I	Branch	B						63-033-1				
	Bran Rel	BR						"				
	Bran Enable	BE						"				
	Bran Disable	BD						(Ind xfr only)				
	Bran Indic.	BI										
	If Not E Box Test											
	1st Level Set Wait	BEW										
II	SIC B	SIC B				X		02-033-1				
		SIC BR				X		(pseudo				
		SIC BE				X		store)				
		SIC BD				X		"				
	Count & Bran	CB						"				
	(If No OPD)	SIC BR			X	X		"				
		CBR										
	(If No OPD)	SIC CBR			X	X						
	(If Not E Box Test)	SIC BIN				X						
	1st Level	SIC BEW				X						
III		SIC B			X			33-073-3				
		SIC BR			X			"				
		SIC BE			X			"				
		SIC BD			X			(real ext				
	(If Not E Box Test)	SIC BI			X			store in				
	1st Level	SIC BEW			X			ECC)				
IV	No Oped	SIC CB				X		02-023-1	02-033-1			
	No Oped	SIC CBR				X		(pseudo store)	(pseudo store)			
V	2nd Level	BEW						00-033-1 (test level)				
VI	3rd Level	BEW						00-023-1 (test level)				

LEVEL AB 10-27-57 WJW

Appendix IV

IAUC LEVEL FUNCTION




OCC LEVEL FUNCTION
NO 1 ERROR
LC LF
0 1
ADV EN SEQ
E OP CHECK
M OP CHECK
ADV EN SEQ
LC i
1 ERROR → NO 2 ERROR
ADV EN SEQ
E OP CHECK
M OP CH
E OP CORRECT
M OP CORR
LC i
1 ERROR → 2 ERROR
ADV EN SEQ
E OP CHECK
M OP CH
E OP CORRECT
M OP COR
LC i
NOOP i
INST REJECT i
LC LF
1 1
ADV EN SEQ ADV EN SEQ
INCLUDES ALL INSTRUCTIONS EXCEPT THOSE WITH EXT ADDRESSES
A+B SAMPLE REFERENCE
LEVEL AB DATE 10-27-59 WCS
PAGE OB

LEVEL FUNCTIONS VFL OP CODE LEVEL

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT OPERATION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	01-003 $\overline{WBC}$ 01-043 WBC	ADV EN SEQ — TBC AES LATE DEC EN E-T TIMER M-T TIMER SAU START DECODE G.O. TOB → E DECODE G.O. OP CODE → E DECODE G.O. WBC → E G1 SAU HSKPING 1ST CYC MEM	01-103 $\overline{WBC}$ 01-143 WBC OR 01-003 $\overline{WBC}$ 01-043 WBC (W) NOOP MODE	ADV EN SEQ — ADV EN SEQ LATE DEC EN — LATE	1ST VFL LEV	ADV EN SEQ T-LA HSCLN MODE IF IRPT ON IMM PREVIOUS INSTR, NORMAL OPER FOR TBC IN GENERAL HOUSECLEAN ACTION WILL FALL INTO THE FOLLOWING CATEGORIES 1) 1ST VFL LEVEL 2) 1ST FLP LEVEL 3) EA BUSY LEVEL 4) PSEUDO STORE LEVEL 5) NONE OF THE ABOVE
ABC	01-003 $\overline{WBC}$ 01-043 WBC	ADV EN SEQ — AES E-IND XFER M-IND XFER DECODE GO ALL INDICATORS & IC G1 $\overline{XR}$ IND MAR NEXT INSTR MAR MODE LA DISABLE IRPT LINE T-SAU EN MEM	01-103 $\overline{WBC}$ 01-103 WBC	ADV EN SEQ — ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC G1 $\overline{XR}$ IND G1 CN IDC LA DISABLE IRPT LINE T-NOOP MODE MAR NEXT INSTR MAR MODE	1ST VFL LEV	ADV EN SEQ — ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC G1 CN IDC IND IRPT THIS INSTR VFL IRPT — VFL INSTR REJ — EXEC UNIT IDLE LA DISABLE IRPT LINE T-LA HSC LN MODE T-IRPT IN H LD RSET I REQ — RSET LA HK REQ I HSCLN REQ — LA HSCLN REQ VFL HKP — VFL NOT OPERATING
SCC	XX-XX3	ADV EN SEQ — ADV EN SEQ RESET LFL A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE

Page 1

LEVEL AB 10-27-59 WCS

VFL ONLY OPER AND $\overline{\text{INT}}$ 1C

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT OPERATION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	05-033	ADV EN SEQ ADV EN SEQ LATE DEC EN E-T TIMER M-T TIMER DECODE GO TOB → C GI TOB → C VFL GO VFL HSKEEPING	05-133 05-033 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE INTERLOCK A-T	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN MODE IF IRPT ON IMM PREVIOUS INSTR, NORMAL OPERATION FOR TBC WILL BE INHIBITED SINCE IT MUST LOOK FOR MAR MODE
ABC	05-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{\text{XR}}$ IND GI BUFF MAR MADE E-IND TEST M-NORM IND TEST SAU EN MEM RESET SAU EN MEM	05-133 05-033 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XPER M-IND XFER DECODE GO ALL IND & IC GI $\overline{\text{XR}}$ IND GI CNIDC GI → BUFF MAR NEXT INSTR MAR MODE MAR MODE T-NOOP MODE RESET PAU MASTER TESTS CMPT E-IND TEST SAU EN MEM M-NOOP TEST RESET SAU EN MEM SAU INSTR REJ SAU HSKPING SAU NOT OPERATING		ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DECODE GO ALL IND & IC GI CNIDC IND LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+PS INT+BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ ADV EN RESET LFL A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE

VFL ONLY OPERAND INT IC

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT OPERATION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	05-037	ADV EN SEQ AES LATE DECODE ENABLE LDE	05-137 05-037 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC ENABLE LATE INTERLOCK A-T	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	05-037	ADV EN SEQ AES E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND GI→BUFF MAR MODE SAU EN MEM EE-A TIMER E-A TIMER M-A TIMER GO INT REG GI→C CHK DATA OR CHK DATA SAU GO RESET EA BUSY SAU HSKPING E-IND TEST M-NORM IND TEST RESET SAU EN MEM	05-137 05-037 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI→BUFF MAR NEXT IN STR MAR MODE MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT RESET EA BUSY SAU INSTR REJ SAU HSKPING SAU NOT OPERATING E-IND TEST M-NOOP TEST RST SAU ENMEM SET NOOPI	EA BUSY LEV	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPI LA DISABLE IRPT LINE T-LA HSCLN MODE IRPT+PS INT+BR REC IN H LOAD
SCC	XX-XX3	ADV EN SEQ ADV EN RESET LFI A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AB 670-60 WCS

VFL ONLY OPERAND $\overline{INT}$ $\overline{IC}$

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT OPERATION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	05-023	ADV EN SEQ ADV EN LATE DEC EN LATE E-TIMER M-T TIMER DECODE GO ToB → C GI ToB → C SAU GO SAU HSKPING	05-123 05-023 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE	NO SPEC ACTION	ADV EN SEQ IF IRPT ON IMM PREVIOUS INST NORMAL OPERATION FOR TBC WILL BE INH'D SINCE IT WILL LOOK FOR MAR MODE T-LA HSCLN MODE
ABC	05-023	ADV EN SEQ ADV EN E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE	05-123 05-023 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CN DC MAR MODE NOOP MODE SAU INSTR REJ SAU HSKPING SAU NOT OPERATING		ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CN DC IND LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT & PS INT & BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ ADV EN RESET LFL A+B SAMPLE REFERENCE	XX-XX3	A & B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

VFL ONLY OPERAND INT $\overline{IC}$

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DISIG	TIMING & INTERLOCKS	LEVEL	TIMING & INTERLOCK
TBC	05-027	ADV EN SEQ AES LATE DEC EN LDE	05-127 05-027 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	05-027	ADV EN SEQ AES E-IND XFER M-IND XFER DECODE GO ALL IND & IC MAR MODE EE-A TIMER GI $\overline{XR}$ IND E-A TIMER M-A TIMER GO INT REG GI→DC CHK DATA OR $\overline{CHR}$ DATA SAU GO RESET EA BUSY SAU HSKPING	05-127 05-027 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE RESET EA BUSY SAU INSTR REJ SET NOOPI SAU HSKPING SAU NOT OPERATING	EA BUSY LEV	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOP LA DISABLE IRPT LINE T-LA HSCLN MODE IRPT + PS INT + BR REC INH LOAD
SCC	XX-XX3	ADV EN SEQ	XX-XX3			

A+B SAMPLE REFERENCE

A+B SAMPLE REFERENCE

A+B SAMPLE REFERENCE

LEVEL AC 1-20-60 WCS Page 5

VFL 1ST OPERAND INT

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	03-023	ADV EN SEQ ADV EN SEQ LATE DECEN LDE E-T TIMER M-T TIMER DEC GO TOB→DC GI TOB→DC	03-123 03-023 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN MODE IF IRPT ON IMM PREVIOUS INST, NORMAL OPERATION FOR TBC WILL BE INHB SINCE IT MUST LOOK FOR MAR MODE
ABC	03-023	ADV EN SEQ ADV EN E-IND XFER M-IND XFER DEC GO ALL IND & IC GI XR IND MAR MODE	03-123 03-023 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI XR IND GI CNIDC MAR MODE NOOP MODE SAU INSTR REJ SAU HSKPING SAU NOT OPERATING		ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER GO ALL IND & IC GI CNIDC IND LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT & PS INT & BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ ADV EN SEQ RESET LFL	XX-XX3			
		A+B SAMPLE REFERENCE		A+B SAMPE REFERENCE		A+B SAMPLE REFERENCE

VFL 1ST OPERAND INT

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	03-027	ADV EN SEQ — AES LATE DEC EN — DE	03-127 03-027 NOOP MODE	ADV EN SEQ — ADV EN SEQ LATE DEC EN — LATE	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	03-027	ADV EN SEQ — AES E-IND XFER M-IND XFER DECODE — GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE EE-ATIMER E-ATIMER M-A TIMER GO INT REG GI→C CHK DATA OR $\overline{CHK}$ DATA RESET EA BUSY	03-127 03-027 NOOP MODE	ADV EN SEQ — ADV EN SEQ E-IND XFER M-IND XFER DEC — GO ALL IND & IC GI $\overline{XR}$ IND GI CN DC MAR MODE NOOP MODE RESET EA BUSY SAU INSTR REJ SET NOOP SAU HSKPING — SAU NOT OPERATING	EA BUSY LEV	ADV EN SEQ — ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC — GO ALL IND & IC GI CN DC IND RESET EA BUSY SET NOOP LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT + PS INT + BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ — ADV EN RESET LF	XX-XX3			
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AA 10-27-59 WCS

VFL 2ND OPER AND INT IC

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	07-037	ADV EN SEQ AES LATE DEC EN LDE	07-137 07-037 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE INTERLOCK A-T	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	07-037	ADV EN SEQ AES E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND GI BUFF MAR MODE EE-A TIMER E-A TIMER M-A TIMER GO INT REG GI→D CHK DATA OR $\overline{CHK}$ DATA SAU GO RESET EA BUSY SAU HSKPING E-IND TEST M-NORMAL IND TEST RESET SAU EN MEM	07-137 07-037 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI→BUFF MAR NEXT INSTR MAR MODE MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT RESET EA BUSY SAU INSTR REJ SAU HSKPING SAU NOT OPERATING E-IND TEST M-NOOP MODE SET NOOP2 RESET SAU EN MEM	EA BUSY LEV	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOP LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+PS INT+BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ ADV EN SEQ RESET LF2 A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AB - 1-20-60 WCS

VFL 2ND OPER AND $\overline{INT}$ $\overline{IC}$

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKERS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	07-023	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC E-T TIMER M-T TIMER DECODE GO TOB→D GI→D SAU GO SAU HSKPING	07-123 07-023 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN MODE
ABC	07-023	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE	07-123 07-023 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE SAU INSTR REJ SAU HSKPING SAU NOT OPER	NO SPEC ACTION	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT & PS INT & BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ ADV EN SEQ RESET LFX	XX-XX3			
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AA 10-27-59 WCS

VFL 2ND OPERAND INT $\overline{IC}$

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	07-027	ADV EN SEQ AES LATE DEC EN	07-127 07-027 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	07-027	ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE EE-A-TIMER E-A TIMER M-A TIMER GO INT REG CHK DATA $\overline{CHK\ DATA}$ GI→D RESET EA BUSY SAU GO SAU HSKPING	07-127 07-027 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE SAU INSTR REJ RESET EA BUSY SET NOOPL SAU HSKPING SAU NOT OPERATING	EA BUSY LEV	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPL LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+ PS INT+ BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AB 10-27-59 WCS

VFL STORE C IC

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	17-033	ADV EN SEQ LATE DEC EN ADV EN SEQ LATE	17-033 NOOP MODE	ADV EN SEQ LATE DEC EN INTERLOCK AT ADV EN SEQ LATE	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	17-033	ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI → BUFF GI $\overline{XR}$ IND MAR MODE LST CYC ST MEM SAU LST CYC ST A EE-A TIMER E-A TIMER M-A TIMER GO C CHK ST DATA GI → LA INT LAAR RESET ST TST RST PAU ST TST RESET LFi RESET EA BSY E-IR TIMER (IF ADDR11) INT LAAR GI INT M-IR TIMER GI A+B (IF ADDR8+9) RESET SAU E-IND TEST EN MEM M-NORM TEST ADV EN SEQ	17-033 NOOP MODE	ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI → BUFF MAR NEXT IN STR MAR MODE MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT RESET EA BUSY SET NOOPi E-IND TEST M-NOOP RESET SAU EN MEM ADV EN SEQ	EA BUSY LEV	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPi LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+PS INT+BR REC) INH LOAD
SCC INT LAAR	XX-XX3	ADV EN SEQ RESET LFi	XX-XX3		XX-XX3	
EXT LAAR XS LAAR	17-032	SEE P.55		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

A+B SAMPLE REFERENCE

LEVEL AC.1-29-60 WCS

VFL STORE C $\overline{IC}$

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	17-023	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE	17-023 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC EN	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	17-023	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE MEM LST CYC STD A EE-A TIMER E-A TIMER M-A TIMER GO C CH ST DATA GI ← LA $\overline{INT}$ LAAR RESET ST. TEST RST PAU ST TEST RESET LFL RESET E A BUSY E-IR TIMER INT LAAR GI INT M-IR TIMER GI A+B (IF ADDR B+9) IF BB, ONE OF 3 RESPONSES SET Ⓦ LST CYC ST (SEE P.26)	17-023 NOOP MODE (IF ADDR 11)	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE RESET E A BUSY SET NOOPL	EA BUSY LEV	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPL LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+PS INT+BR REC) INH LOAD
SCC INT LAAR	XX-XX3	ADV EN SEQ ADV EN SEQ RESET LFL	XX-XX3		XX-XX3	
EXT LAAR XS LAAR	17-022	SEE PAGE 55 A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AB 1-29-60 WCS

VFL STORE D IC

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	23-033	ADV EN SEQ ADV EN SEQ LATE DECODE EN LATE DEC EN	23-033 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE INTERLOCK A-J	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	23-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-INDXFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND GI → BUFF MAR MODE LST CYC ST MEM EE-A TIMER E-A TIMER M-A TIMER GO D CHK ST DATA GI → LA $\overline{INT}$ LAAR RESET ST TEST RST PAU ST TEST RESET LFL RESET EA BUSY E-IR TIMER INT LAAR GI INT M-IR TIMER GI A+B (IF ADDR B+9) E-IND TEST RESET SAU EN MEM M-NORM TEST	23-033 NOOP MODE (IF ADDR 1)	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI → BUFF MAR NEXT INSTR MAR MODE MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT RESET EA BUSY SET NOOPL E-IND TEST M-NOOP TEST RESET SAU EN MEM	EA BUSY LEV	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPL LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+PS INT+BR REC) INH LOAD
SCC INT LAAR	XX-XX3	ADV EN SEQ RESET LFL A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE
EXT LAAR IND LAAR	23-032	SEE P. 55				

LEVEL AB 1-29-60 WCS

VFL STORE D TC

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	23-023	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC	23-023 NOOP MODE	ADV EN SEQ LATE DEC EN LATE DEC EN	EA BUSY LEV	ADV EN SEQ T-LA HSCLN MODE
ABC	23-023	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI XR IND MAR MODE LAST CYC STORE MEM EE-A TIMER E-A TIMER M-A TIMER GO D CHK ST DATA GI→LA INT LAAR RESET ST TEST RESET PAU ST TEST RESET LFL RESET EA BUSY E-IR TIMER INT LAAR GI INT M-IR TIMER GI A+B (IF ADDR B+9)	23-023 NOOP MODE (IF ADDR 11)	ADV EN SEQ ADV EN SEQ E-IND X FER M-IND XFER DEC GO ALL IND & IC GI XR IND GI CN IDC MAR MODE NOOP MODE RESET EA BUSY SET NOOP1	EA BUSY LEVEL	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOP1 LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+PS INT+BR REC) INH LOAD
SCC INT LAAR	XX-XX3	ADV EN SEQ RESET LFL	XX-XX3			
EXT LAAR XS LAAR	23-022	SEE P. 55				
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AB 1-29-60 WCS

VFL STORE BUS IC NORMAL TERMINATION

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING INTERLOCKS	LEVEL DESIG	TIMING INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	21-033	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC EN	21-033 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE INTERLOCK A-T	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	21-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND GI → BUFF MAR MODE LST CYC STORE MEM A E-A TIMER M-A TIMER UNLATCH BUS GI LA INT LAAR { RESET ST TEST; RESET RST LFi PAU ST TST } E-I R TIMER (IF ADDR 11) INT LAAR { STEA BUSY GI INT; M-IR TIMER; GIA+B (IF ADDR 8+9) } E-IND TEST M-NORM TEST RESET SAU EN MEM	21-033 NOOP MODE	ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI → BUFF MAR NEXT INSTR MAR MODE MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT RESET EA BUSY SET NOOPi E-IND TEST E-NOOP TEST RESET SAU EN MEM	EA BUSY LEVEL	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPi LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT + PS INT + BR REC) INH LOAD
SCC INT LAAR	XX-XX3	ADV EN SEQ RESET LFi				
EXT LAAR XS LAAR	21-032	SEE P. 55				
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AB 1-29-60 WCS

VFL STORE BUS IC NO STORE DUE TO DZ

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	21-033	ADV EN SEQ ADV EN SEQ TBC DEC ADV REGARDLESS OF NOOP LATE LATE DEC EN	21-033 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE INTERLOCK A-T	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	21-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND GI → BUFF MAR MODE MEM THIS STORE INHD E-A TIMER M-A TIMER RESET EA BUSY E-IND TEST M-NORM TEST NOOP↓ RESET SAU EN MEM		ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI → BUFF MAR NEXT INSTR MAR MODE MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT RESET EA BUSY SET NOOP↓ E-IND TEST M-NOOP TEST RESET SAU EN MEM	EA BUSY LEVEL	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOP↓ LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+PS INT+ BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ ADV EN SEQ RESET LF↓	XX-XX3		XX-XX3	
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

VFL STORE BUS $\overline{IC}$ NORMAL TERMINATION

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	21-023	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC EN	21-023 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DC EN LATE DEC EN	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	21-023	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE (1) MEM LAST CYC STORE E-A TIMER M-A TIMER UNLATCH BUS GI-LA $\overline{INT}$ LAAR { RESET ST TEST RST PAU ST RESET LFi TST E-IR TIMER(IFADDR11) INT LAAR { RESET EA BUSY GI INT M-IR TIMER GI → A+B (IF ADDR B+9)	21-023 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE RESET EA BUSY SET NOOPi	EA BUSY LEV	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPi LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+ PS INT+ BR REC) INH LOAD
SCC INT LAAR	XX-XX3	ADV EN SEQ RESET LFi	XX-XX3			
EXT LAAR XS LAAR	21-022	SEE P. 55				
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AB 1-29-60 WCS

VFL STORE BUS $\overline{IC}$ NO STORE DUE TO DF

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	21-023	ADV EN SEQ LDE LATE DEC EN TBC DEC ADV INDEPENDENT OF NOOPL	21-023 NOOP MODE	ADV EN SEQ LDE LATE DEC EN	EA BUSY LEV	ADV EN SEQ T-LA HSCLN MODE
ABC	21-023	ADV EN SEQ ADV EN SEQ E-IND-XFER M-IND-XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE THIS STO IN HD MEM A E-A TIMER M-A TIMER RESET EA BUSY NOOPL	21-023 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GIC NIDC MAR MODE NOOP MODE RESET EA BUSY SET NOOPL	EA BUSY LEVEL	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPL LA DISABLE IRPT LINE T-LA HSCLN MODE IRPT+ PS INT+ BR REC INH LOAD
SCC	XX-XX3	ADV EN SEQ AES RESET LFL	XX-XX3		XX-XX3	
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AB. 10-27-59 WCS Page 19 Lee

VFL MPYC OPER AND IC

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSE CLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	15-033	ADV EN SEQ ADV EN SEQ LATE DEC EN GO TOB→DC DECODE SAU RDY FOR MEM MPYC OPND E-T TIMER M-T TIMER GI→DC NO VFL WAIT FOR OPER AND GI RES→CHKR	15-133 15-033 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE INTERLOCK A-T	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN MODE
ABC	15-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND GI→BUFF MAR MODE E-IND TEST M-NORM TEST RESET SAU EN MEM	15-133 15-033 NOOP MODE	ADV-EN-SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI→BUFF MAR NEXT INSTR MAR MODE MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT SAU INSTR REJ VFL NOT OPER E-IND TEST M-NOOP RESET SAU TEST EN MEM	NO SPEC ACTION	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT & PS INT & BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ AES RESET LFL A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AC 1-29-60 WCS

VFL MPYC OPERAND $\overline{IC}$

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		INTERRUPT ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	15-023	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC DEC GO TOB → C SAU RDY FOR MPYC MEM OPER AND E-T TIMER M-T TIMER GI → C NO SAU WAIT FOR OPERAND GI RES → CHKR	15-123 15-023 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC EN	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN MODE
ABC	15-023	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE	15-123 15-123 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE SAU INSTR REJ SAU NOT OPERATING	NO SPEC ACTION	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT & PS INT & BR REC) INH LOAD
SEE	XX-XX3	ADV EN SEQ RESET LFL	XX-XX3			
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AA 10-27-59 WCS

NORMAL CODE FOR VFL PX LEVEL

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		INTERRUPT ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	04-033	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC EN	04-033 NOOP MODE	ADV EN SEQ AES LATE DEC EN INTERLOCK A-T	PSEUDO STORE	ADV EN SEQ T-LA HSCLN MODE
ABC	04-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DECODE GO ALL IND & IC GI $\overline{XR}$ IND GI → BUFF GI XR IND LST CYC ST MEM MAR MODE E-IND TEST M-NORM TEST RESET SAU EN MEM	04-033 NOOP MODE	ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI BUFF MAR NEXT INSTR MAR MODE MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT SET PS INT INH LOAD RESET LFL E-IND TEST M-NOOP TEST I HSCLN REQ T-LA HSCLN MODE RST I REQ LA HK REQ RESET SAU EN MEM RST LA REQ	PSEUDO STORE	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET LFL LA DISABLE IRPT LINE T-IRPT INH LOAD T-LA HSCLN MODE
SCC	XX-XX3	ADV EN SEQ RESET LFL A+B SAMPLE REFERENCE	04-032	SEE P. 58 A+B SAMPLE REFERENCE	04-032	SEE P. 58 A+B SAMPLE REFERENCE

NOOP CODE FOR VFL PX LEVEL

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSE CLEAN ACTION	
	LEVEL DESIG.	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	06-033	ADV EN SEQ ADV EN SEQ LATE DEC ENABLE	04-033 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN INTERLOCK A-T	PSEUDO STORE	ADV EN SEQ T-LA HSCLN MODE
ABC	06-033	ADV EN SEQ E-IND XFER M-IND XFER DEL GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI → BUFF LST CYC MEM MAR MODE SET PS INT INH LOAD RESET LF2 I BOX HSCLN REQ T-LA-HSCLN RST I REQ LA HSCLN REQ E-IND-TEST RST LA REQ M-NORMAL TEST RESET SAU EN MEM	04-033 NOOP MODE	ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & TC GI $\overline{XR}$ IND GI CNIDC GI → BUFF MAR NEXT INSTR. MAR MODE MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT SET PS INT INH LOAD RESET LF2 I BOX HSCLN REQ T-LA-HSCLN MODE RST I REQ LA HKLN REQ E-IND TEST RST LA REQ M-NOOP TEST RESET SAU EN MEM	PSEUDO STORE	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET LF2 LA DISABLE IRPT LINE T-IRPT INH LOAD TA-LA HSCLN MODE
SCC	06-032	SEE P. 58 A+B SAMPLE REFERENCE	06-032	SEE P. 58 A+B SAMPLE REFERENCE	06-032	SEE P. 58 A+B SAMPLE REFERENCE

VFL OP CODE LEVEL INDICATOR BRANCH

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	35-023	ADV EN SEQ — ADV EN SEC LATE DEC EN — LDE E-T TIMER M-T TIMER DEC GO TOB → E DEC GO OP CODE → DE DEC GO WBC → DE DEC GO VFL IB → DE SAU START GI — SAU HSKPING 1ST CYC MEM	35-123	ADV EN SEQ — ADV EN SEQ LATE DEC EN — LATE	1ST VFL LEV	ADV EN SEQ — IF IRPT ON IMM PREVIOUS INSTR NORMAL OPER FOR TBC T-LA HSCLN MODE IN GENERAL HOUSECLEAN ACTION WILL FALL INTO THE FOLLOWING CATEGORIES 1) 1ST VFL LEVEL 2) 1ST FLP LEVEL 3) EA BUSY LEVEL 4) PSEUDO STORE LEVEL 5) NONE OF THE ABOVE
ABC	35-023	ADV EN SEQ — ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND MAR NEXT INSTR MAR MODE T-SAU EN MEM	35-123	ADV EN SEQ — ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC CI $\overline{XR}$ IND CI CNIDC MAR NEXT INSTR MAR MODE NOOP MODE	1ST VFL LEV	ADV EN SEQ — ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND IRPT THIS INSTR VFL IRPT — VFL INSTR — EXEC REJ — UNIT — IDLE LA DISABLE IRPT LINE LA HSC LN MODE T-IRPT INHLD RSTI REG — RST LA REQ IHS CLN REQ — LA HSCLN REQ VFL HKP — VFL NOT OPERATING
SCC	XX-XX3	ADV EN SEQ — AES RESET LFi	XX-XX3		XX-XX3	
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

VFL 1B OPERAND INT $\overline{IC}$

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSESCLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS		TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	37-027	ADV EN SEQ AES LATE DC EN	37-127 37-027 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE	EA BUSY LEVEL	ADV EN SEQ IF IRPT ON IMM PREVIOUS INSTR NORMAL OPERATION FOR TBC WILL BE NH SINCE IT MUST LOOK FOR MAR MODE T-LA HSCLN MODE
ABC	37-027	ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND EE-A TIMER EA TIMER M-A TIMER GO IND REG GI→C CHK DATA SAU GO SAU HSKPING MAR MODE RST IND REG 00-19	37-127 37-027 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE SAU INSTR REJ RESET EA BUSY SET NOOPi SAU HSKPING SAU NOT OPERATING	EA BUSY LEVEL	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPi LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT & PS INT & BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ	XX-XX3			
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

VFL IB STORE C

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSE CLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	41-023	ADV EN SEQ ADV EN SEQ LATE DEC EN LDE	41-023 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC EN	EA BUSY LEVEL	ADV EN SEQ IF IRPT ON IMM PREVIOUS INSTR NORMAL OPERATION FOR TBC WILL BE INHIB'D SINCE IT MUST LOOK FOR MAR MODE T-LA HSCLN MODE
ABC	41-023	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE LST CYC STORE MEM (1) BR SUCC · $\overline{COND}$ IND MEM (2) BR SUCC · COND IND MEM (3) BR UNSUCC MEM EE-A TIMER E-A TIMER M-A TIMER GO C REG CHK ST DATA GI INT REG GI-0-19 RESET EA BUSY	41-023 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE	EA BUSY LEVEL	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOP'S LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT & PS INT & BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ RESET LFL A+B SAMPLE REFRENCE	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

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VFL BB OPCODE LEVEL

COUNTER	NORMAL OPERATION LEVEL DESIG	NORMAL OPERATION TIMING & INTERLOCKS	INSTRUCTION REJECT ACTION LEVEL DESIG	INSTRUCTION REJECT ACTION TIMING & INTERLOCKS	HOUSECLEAN ACTION LEVEL DESIG	HOUSECLEAN ACTION TIMING & INTERLOCKS
TBC	43-023	ADV EN SEQ ADV EN SEQ LATE DEC E-T TIMER M-T TIMER DEC GO ToB→E DEC GO OP CODE→E DEC GO WBC→E DEC GO VFL BB→E SAU START GI SAU HSKPING 1ST CYC MEM	41-123	ADV EN SEQ ADV EN SEQ LATE DEC ENABLE LATE	1ST VFL LEV	ADV EN SEQ IF IRPT ON IMM PREVIOUS INSTR NORMAL OPERATION FOR TBC T-LA HSCLN MODE IN GENERAL HOUSECLEAN ACTION WILL FALL INTO THE FOLLOWING CATEGORIES: 1) 1ST VFL LEVEL 2) 1ST FLP LEVEL 3) EA BUSY LEVEL 4) PSEU STORE LEVEL 5) NONE OF THE ABOVE
ABC	43-023	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE T-SAU EN MEM	41-123	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER GO ALL IND & IC GI XR IND GI CNIDC MAR MODE NOOP MODE	1ST VFL LEV	ADV EN SEQ E-HSCLN TIMER M-HSCLH TIMER DEC GO ALL IND & IC GI CN IC IND IRPT THIS INSTR VFL IRPT VFL INSTR REJ EX EC UNIT IDLE LA DISABLE IRPT LINE T-LA HSC LNMODE T-IRPT INH LD R SET LA NK REQ RSET I REQ I HSCLN REQ LA HSCLN REQ VFL HKP VFL NOT OPERATING
SCC	XX-XX3	ADV EN SEQ RESET LFL A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

VFL IB OR BB RECOVERY LEVEL

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	45-033	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC EN	45-033 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE INTERLOCK (A-T)	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN MODE
ABC	45-033	ADV EN SEQ RESPONSE (1) ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI XR IND GI BUFF MAR MODE M-BR SUCC COND IND RESET LFL T-BR RECOVERY INH LOAD E-IND TEST M-NORM TEST RST LA REQ I BOX HSKPN REQ T-LA HK MODE RSET I HK REQ LA HSKLN REQ SCC SEES 45-032 P.56	45-033 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI XR IND GI CNIDC GI BUFF MAR MODE MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT E-IND TEST M-NOOP TEST	NO SPEC ACTION	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT & PS INT & BR REC) INH LOAD
		ADV EN SEQ ADV EN SEQ RESPONSE (2) E-IND XFER M-IND XFER DEC GO ALL IND & IC GI XR IND GI BUFF MAR MODE M-BR SUCC COND IND GI COND IND FR EXEC REG E-IND TEST M-NORM TEST SCC SEES XX-XX3				
		ADV EN SEQ ADV EN SEQ RESPONSE (3) E-IND XFER M-IND XFER DEC GO ALL IND & IC GI XR IND GI BUFF MAR MODE M-BR UNSUCCESSFUL E-IND TEST M-NORM TEST SCC SEES XX-XX3				
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

NOOP CODE FOR IB OR BB RECOVERY LEVEL

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	47-033	ADV EN SEQ ADV EN SEQ LATE DEC . LATE DEC EN EN	47-033 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC ENABLE LATE	NO SPEC ACTION	ADV EN SEQ IF IRPT ON IMM PREVIOUS INSTR, NORMAL OPERATION FOR TBC WILL BE INH'D T-LA HSCLN SINCE IT MUST LOOK FOR MAR MODE MODE
ABC	47-033	ADV EN SEQ RESPONSE (1) E-IND XFER M-IND XFER DEC GO ALL IND & IC GI XR IND GI CNIDC GI BUFF MAR MODE M-BR SUCC. COND IND E-IND TEST M-NORMAL TEST	47-033 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO IND & IC GI XR IND GI CNIDC GI BUFF MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT E-IND TEST M-NOOP TEST	NO SPEC ACTION	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT & PS INT & BR REC) INH LOAD
		ADV EN SEQ ADV EN SEQ RESPONSE(2) E-IND XFER M-IND XFER DEC GO ALL IND & IC GI XR IND GI CNIDC SCC SEES XX-XX3 GI BUFF MAR MODE M-BR SUCC COND IND GI COND IND E-IND TEST M-NORM TEST				
		ADV EN SEQ AES RESPONSE (3) E-IND XFER M-IND XFER DEC GO ALL IND & IC SCC SEES XX-XX3 GI XR IND GI BUFF MAR MODE M-BR UNSUCCESS E-IND TEST M-NORM TEST	XX-XX3			
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

VFL STICA-IB RECOVERY LEVEL (I BOX WAITING FOR LA RESPONSE 1) RESUME - STICA OR 2) RESUME - NO STICA)

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	45-023	ADV EN SEQ ADV EN SEQ LATE DEC LDE EN	45-023 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC LDE EN	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN
ABC	45-023	RESPONSE (1) ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE M-BR SUCC COND IND RESUME-STICA	45-023 NOOP MODE	ADV EN SEQ AES E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE RESUME-NO STICA		ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND LA DISABLE IRPT LINE T-LA HSCLN (IRPT & PS INT & BR REC) INH LOAD
		RESPONSE (2) ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE M-BR SUCC COND IND RESUME-NO STICA GI COND IND FR EXEC REQ				
		RESPONSE (3) ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND MAR MODE M-BR UNSUCCESSFULL RESUME-NO STICA				
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AA 10-27-59 WCS

SINGLE LEVEL FL PT $\overline{\text{INT}}$ S

COUNTER	NORMAL OPERATION		INSTRUTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	02-013	ADV EN SEQ ADV EN SEQ LATE DEC EN LDE E-T TIMER M-T TIMER DEC GO TOB → C DEC GO OP CODE → E FLP GI OC & ST FLP GI TOB → C PAU GI 1ST MEM CYCLE (T_0)	02-113	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE INTERLOCK A-T	1ST FLP LEV	ADV EN SEQ IF IRPT ON IMM PREVIOUS INSTR NORMAL OPERATION HERE T-LA HOUSECLEAN MODE
ABC	$\overline{011}$-02-013	ADV EN SEQ ADV EN SEQ E IND XFER M IND XFER DEC GO ALL IND & IC GI $\overline{\text{XR}}$ IND GI → BUFF E IND TEST RESET LA MAR MODE M-NORM TEST LA MAR MODE	$\overline{011}$-02-113	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{\text{XR}}$ IND GI CNIDC GI → BUFF NOOP MODE RESET PAU MASTER TESTS CMPT E-IND TEST RESET LA MAR MODE M-NOOP TEST MAR MODE		ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC FLP SET EXEC IDLES T-IRPT INH LOAD I BOX HSCLN REQ T-LA HSCLN MODE RSET I HSCLN REQ LA HSCLN REQ RESET IRPT NEXT INSTR RSET LA HK REQ T-LA DISABLE IRPT
SCC	XX-XX3	ADV EN SEQ RESET LFL	XX-XX3			
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

SINGLE LEVEL FLP INT 3

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	02-017	ADV EN SEQ ADV EN SEQ LATE DEC EN GI 1ST CYC MEM (T_0) DEC GO OP CODE → E	02-117	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC INTERLOCK A-T	EA BUSY LEV	ADV EN SEQ T-LA HSCLN MODE
ABC	$\overline{011}$-02-017	ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI → BUFF EE-A TIMER E-A TIMER M-A TIMER GO INT REG GI ACOB → C FLP GI OC & ST CHK DATA OR $\overline{CHK}$ DATA RESET EA BUSY E-IND TEST RESET LA MAR MODE M-NORM TEST LA MAR MODE	$\overline{011}$-02-117	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNID C GI → BUFF NOOP MODE RESET PAU MASTER TESTS CMPT RESET EA BUSY E-IND TEST RESET LA MAR MODE M-NOOP LA MAR MODE TEST SET NOOPi	EA BUSY LEVEL	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPi LA DISABLE IRPT LINE T-LA HSCLN MODE IRPT + PS INT + BR REC IN A LOAD
SCC	XX-XX3	ADV EN SEQ A&B SAMPLE REFERENCE	XX-XX3	A&B SAMPLE REFERENCE		A&B SAMPLE REFERENCE

FL. PT. 1ST LEV. INT

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	IG	TIMER & INTERLOCKS
TBC	02-003	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC E-T TIMER M-T TIMER DEC GO TOB → C DEC GO OP CODE → E FLP GI OC & CT FLP GI TOB & C GI 1ST CYC MEM (To)	02-103	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC	1ST FLP LEV	ADV EN SEQ T-LA HOUSECLEAN MODE
ABC	02-003	ADV EN SEQ ABC ADV E IND XFER M IND XFER DEC GO ALL IND & IC GI XR IND LA MAR MODE	02-103	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI XR IND GI CNIDC LA MAC MODE NOOP MODE		ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND EXEC IDLES FLP SET T-IRPT INH LOAD I BOX HSCLN REQ T-LA HSKLN MODE RESET I HSCLN REQ LA HSKLN REQ RESET IRPT NEXT INSTR RESET LA HK REQ T-LA DISABLE IRPT
SCC	XX-XX3	ADV EN SEQ AES RESET LFL	XX-XX3			
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

FL PT 1ST LEVEL INT

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCK
TBC	02-007	ADV EN SEQ ADV EN LATE DEC EN LDE GI 1STCYC MEM DEC GO OP CODE → E (To)	02-107	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	02-007	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND LA MAR MODE EE-A TIMER E-A TIMER M-A TIMER GO INT REG GI ACOB → C FLP GI OC & ST CHK DATA OR CHK DATA RESET EA BUSY	02-107	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC LA MAR MODE NOOP MODE RESET EA BUSY SET NOOPi	EA BUSY LEVEL	ADV EN SEQ, AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPi LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+PS INT+BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

FLP 2ND LEV STORE BUS NORMAL TERMINATION

COUNTER	NORMAL OPERATION LEVEL DESIG	NORMAL OPERATION TIMING & INTERLOCKS	INSTRUCTION REJECT ACTION LEVEL DESIG	INSTRUCTION REJECT ACTION TIMING & INTERLOCKS	HSCLN ACTION LEVEL DESIG	HSCLN ACTION TIMING & INTERLOCKS
TBC	13-033	ADV EN SEQ ADV EN SEQ TBC DEC ADV MUST BE INDEPENDENT OF NOOPL LATE DEC EN LATE	13-033 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC ENABLE LATE DEC INTERLOCK A-T	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	13-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI→BUFF (1) LST CYC ST MEM E-A TIMER M-A TIMER UNLATCH BUS GI→LA DELAY ADV AGAIN IF ADDR II INVOLVED INT LAAR: RESET ST TEST; ADV ON M IND REG TIMER; RESET FLP; RESET LFL INT LAAR: ST TST RPT EA BUSY; GI→INT; E-IND REG TIM; M-IR TIM; (IF ADDR B+19) GI A+B; IR→UIR; E-IND TEST LA MAR MODE M-NORM TEST MAR MODE	13-033 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI→BUFF NOOP MODE RESET PAU MASTER TESTS CMPT RESET EA BUSY SET NOOPL E-IND TEST LA MAR MODE M NOOP TEST MAR MODE	EA BUSY LEV	ADV EN SEQ E-HSCLN TIMER AES M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPL LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+PS INT+BR REC) INH LOAD
SCC INT LAAR	XX-XX3	ADV EN SEQ RESET LFL	XX-XX3			
EXT LAAR XS LAAR	13-032	SEE P. 55				
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AB 1-29-60 WCS

FLP 2ND LEV STORE BUS NO STORE TO DZ IND

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEANING ACTION	
	LEVEL DESIG	TIMING INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCK
TBC	13-033	ADV EN SEQ ADV EN SEQ TBC DEC ADV MUST BE INDEPENDENT ON NOOP; LATE DEC EN	13-033 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC ENABLE LATE DEC INTERLOCK A-T	EA BUSY LEVEL	ADV EN SEQ T-LA HSCLN MODE
ABC	13-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI→BUFF (2) NO ST DATA MEM E A TIMER M A TIMER RESET EA BUSY E-IND TEST LA MAR MODE M-NORMTEST NOOP;	13-033 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI→BUFF NOOP MODE RESET PAU MASTER TESTS CMPT RESET EA BUSY SET NOOP; E IND TEST LA MAR MODE M- MAR MODE NOOP TEST	EA BUSY LEV	ADV EN SEQ AES E HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOP; LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+PS INT+BR REC)INH LOAD
SCC	XX-XX3	ADV EN SEQ RST LF;	XX-XX3			
		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AC 1-29-60 WCS

FLP MPYC OPERAND

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HSCLN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	11-033	ADV EN SEQ ADV EN SEQ LATE DEC EN E-T TIMER M-T TIMER DECODE GO TO B → C FLP CONT FLP GI TO B-C GI INTM CYCLE MEM ◁—▷	11-133 11-033 NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE INTERLOCK A-T	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN MODE
ABC	11-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI → BUFF E-IND TEST MAR MODE M-NORM TEST	11-133 11-033 NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI → BUFF NOOP MODE FLP INSTR REJ RESET PAU MASTER TESTS CMPT E-IND TEST LA MAR MODE M-NOOP TEST MAR MODE	NO SPEC ACTION	ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT & PS INT & BR REC) INH LOAD
SCC	XX-XX3	ADV EN SEQ RESET LFL A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

SINGLE LEVEL FLP STORE

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HSCLN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	02-013	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE E-T TIMER M-T TIMER DEC GO TO B→C DEC GO OP CODE→E FLP GI OC & ST FLP GI TO B→C GI 1ST CYC MEM (T0)	02-113	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE INTERLOCK A-T		ADV EN SEQ T-LA HSCLN IF IRDT DUE TO IMM PREV INSTR, NORMAL ACTION HERE
ABC	011-02-013	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI → BUFF LST CYC ST LST CYC ST MEM E-A TIMER RSET LA MAR MODE M-A TIMER UNLATCH BUS GI → LA INT LAAR { RESET ST TST RESET FLP ST RST TEST LF: IND REG TIME INT LAAR { RESET EA BUSY GI→INT M-IR TIM (IF ADDR B+9) GI→A+B IR→UIR E-IND TEST M-NORM TEST	(IF ADDR10	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI → BUFF NOOP MODE RESET PAU MASTER TESTS RESET EA BUSY SET NOOPi E-IND TEST M-NOOP MAR MODE TEST RESET LA MAR MODE	EA BUSY LEV 1ST FLP LEV NOOPED INT CMPT	ADV EN SEQ ADV EN E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPi FLP SET EXEC IDLE'S T-IRPT INH LOAD I BOX HSCLN REQ B T-LA HSCLN MODE RESET I REQ LA HSCLN REQ RSET LA REQ
SCC INT LAAR EXT LAAR XS LAAR	02-012	ADV EN SEQ RESET LF: SEE P.55 A&B SAMPLE REFERENCE	XX-XX3	A&B SAMPLE REFERENCE	XX-XX3	A&B SAMPLE REFERENCE

LEVEL AC 1-29-60 WCS

I BOX STORE INTERNAL $\overline{I.C.}$

	NORMAL OPERATION		INSTR REJECT ACTION		HOUSECLEAN ACTION	
	LEV DESCRIP	TIMING & INTERLOCKS	LEV DESIG	TIMING & INTERLOCKS	LEV DESIG	TIMING & INTERLOCKS
TBC	33-023 LAAR DEC INT	ADV EN SEQ ADV EN SEQ LATE DEC EN INTLK T-A E-T TIMER M-T TIMER GI-C DEC GO TOB → C	33-123 OR 33-023 @ NOOP MODE	ADV EN SEQ LATE DEC EN	EA BUSY LEV	ADV EN SEQ T-LA HSCLN MODE
ABC	33-023 + INTERNAL ADD	ADV EN SEQ ADV EN SEQ INTERLOCK E-IND XFER M-IND XFER EE-A TIMER E-A TIMER M-A TIMER MAR MODE MAR MODE GO C GI $\overline{XR}$ IND GI XR IND DEC GO ALL IND & IC GI INT RESET EA BUSY CHK STO DATA GI A+B (IF ADDR 8+9) E-IND TIMER (IF ADDR 11) M-IND REG TIMER IR → UIR A+B SAMPLE REFERENCE	33-123 OR 33-023 @ NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE RESET EA BUSY SET NOOPL A+B SAMPLE REFERENCE	EA BUSY LEV	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOPL LA DISABLE IRPT LINE T-LA HSCLN MODE IRPT + PS INT + BR REC IN A LDAD A+B SAMPLE REFERENCE
SCC		SEES XX-XX3				

I BOX STORE INTERNAL I.C.

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT		HOUSE CLEAN ACTION	
	LEVEL DESIG.	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	33-033 LAAR DEC INT	ADV EN SEQ ADV EN SEQ LATE DEC EN INTLK TA ET TIMER M-T TIMER GI←C GO TO B←C DEC	33-133 OR 33-033 AT NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC ENABLE INTERLOCK ABC	EA BUSY LEV	ADV EN SEQ T-LAHSCLN MODE
ABC	33-033 LAAR DEC INT	ADV EN SEQ ADV EN SEQ INTERLOCK E-IND XFER M-IND XFER EE-A TIMER E-A TIMER M-A TIMER MAR MODE GO C GI $\overline{XR}$ IND GI XR IND DEC GO ALL IND & IC GI BUFF GI INT RESET EA BUSY RSTPAU CH'K ST DATA MASTER TEST CMPT GI A+B (IF ADDER B+9) EIND REG TIMER (IF ADDR 1) M-IND REG TIMER IR←UIR IR←UIR E-IND TEST M-NOOP TEST	33-133 OR 33-133 AT NOOP MODE	ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND+IC GI $\overline{XR}$ IND GI CNIDC GI BUFF MAR MODE MAR MODE NOOP MODE RESET PAU MASTER TESTS CMPT PS IRPT INH LOAD E-IND TEST M-NOOP TEST I BOX HSCLM REQ T-LA HSCLM MODE RESET I HKLN REQ LA HKLN REQ RESET LA REQ RESET EA BUSY SET NOOP i	EA BUSY LEV	ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC RESET EA BUSY SET NOOP i LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT-PS INT+BR REC) INH LOAD
SCC		SEE XX-XX3				
		A←B SAMPLE REFERENCE		A←B SAMPLE REFERENCE		A←B SAMPLE REFERENCE

I BOX STORE EXTERNAL $\overline{IC}$

	NORMAL OPERATION		INSTR REJECT ACTION		HOUSE CLEAN ACTION	
	LEVEL DESCR	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	33-063 (W) EXT ADDR 33-023 (W) EXT ADDR	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC EN	33-163 OR 33-063 (W) NOOP MODE OR 33-123 OR 33-023 (W) NOOP MODE	ADV EN SEQ LATE DEC EN	EA BUSY LEV	ADV EN SEQ T-LA HSCLN MODE
ABC	33-063 & EXT ADDRESS NOTE: 0+4 CONSIDERED INTERNAL	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER SET $\overline{LF}$ DEC GO ALL IND & IC GI $\overline{XR}$ IND GI XR IND MAR MODE RESET TBC AES	33-123 OR 33-023 (W) NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE RESET EA BUSY SET NOOP i	EA BUSY LEV	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOP i LA DISABLE IRPT LINE T-LA HSCLN MODE IRPT + PS INT + BR REC IN A LOAD
ABC	33-023 & EXT ADDRESS	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER SET $\overline{LF}$ DEC GO ALL IND & IC GI $\overline{XR}$ IND GI XR IND MAR MODE RESET TBC AES RESET LAST CHK TEST	33-123 OR 33-023 (W) NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC MAR MODE NOOP MODE RESET EA BUSY SET NOOP i	EA BUSY LEV	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOP i LA DISABLE IRPT LINE T-LA HSCLN MODE IRPT + PS INT + BR REC IN A LOAD
SCC	33-062 33-022	SEE P. 57 SEE P. 55 A+B SAMPLE REFERENCE		SCC SEES XX-XX3 A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

I BOX STORE EXTERNAL I.C.

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC 33-073 @EXT ADD 33-033 @EXT ADD		SAME AS 33-023	33-173 OR 33-073 @NOOP MODE OR 33-133 OR 33-033 @ NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC ENABLE INTERLOCK ABC	EA BUSY LEV	ADV EN SEQ T-LA HSCLN MODE
ABC 33-073 @EXT ADD		SAME AS 33-063 @EXT ADD G1-IC→BUFF E-IND TEST M NOOP TEST MODE MAR MODE MAR RESET PAU MASTER TEST CMPT	33-173 33-073 NOOP MODE	ADV EN SEQ E-IND XFE M-IND XFER DEC GO ALL IND+IC G1 XR IND G1 CN IDC G1 BUFF MAR MODE MAR MODE NOOP MODE RESET FP PAU MASTER TEST CMPT PS IRPT INH LOAD E-IND TEST M-NOOP TEST T-LA HSCLN MODE IBOX HSCLN REQB RESET I HSCLN REQ LA HKLN REQ RESET EA BUSY RESET LA REQ SET NOOPi	EA BUSY LEV	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND+IC G1 CN1 DC IND RESET EA BUSY SET NOOPi LA DISABLE IRPT LINE T-LA HSCLN MODE IRPT+PS INT+BR REC INH LOAD
ABC 33-033 @EXT ADD		SAME AS 33-023 @EXT ADD G1-IC→BUFF T-IND TEST M-NOOP TEST MODE MAR MODE MAR RESET PAU MASTER TEST CMPT	33-133 33-033 NOOP MODE	ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND+IC G1 XR IND G1 CN IDC G1 BUFF MAR MODE MAR MODE NOOP MODE RESET FP PAU MASTER TEST CMPT PS IRPT INH LOAD E-IND TEST M-NOOP TEST T-LA HSCLN MODE IBOX HSCLN REQB RESET I HSCLN REQ LA HKLN REQ RESET EA BUSY RESET LA REG SET NOOPi		ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND+IG G1 CN1 DC IND RESET EA BUSY SET NOOPi LA DISABLE IRPT LINE T-LA HSCLN MODE IRPT+PS INT+BR REC INH LOAD
SCC 33-072 33-032		SEE P.57 SEE P.55 A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

STICA-BIN STORE (ASSUMED EXTERNAL) IC

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS				
TBC	31-073	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC EN		DOES NOT APPEAR		DOES NOT APPEAR
ABC	31-073	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER SET $\overline{LF}$ E-IND TEST M-NORM TEST MAR MODE RESET TBC AES DEC GO ALL IND $\overline{EIC}$ GI $\overline{XR}$ IND GI BUFF RESET SAU EN MEM		DOES NOT APPEAR		DOES NOT APPEAR
SCC	31-072	SEE P. 57 A+B SAMPLE REFERENCE				

I BOX INDICATOR TRANSFER IC

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING AND INTERLOCKS
TBC	63-033	ADV EN SEQ ADV EN SEQ LATE DEC EN	63-133 OR 63-033@ NOOP MODE	ADV EN SEQ LATE DEC ENABLE LDE INT LK A-T	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN MODE
ABC	63-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER E-IND TEST NOOP M-TEST MAR MODE MAR MODE TBC RESET AES PAU MASTER TESTS RESET DEC GO ALL IND & IC GI $\overline{XR}$ IND GI XR IND GI BUFF	63-133 OR 63-033@ NOOP MODE CMPT	ADV EN SEQ AES E-IND XFER M-IND XFER DEC GO ALL & IC GI $\overline{XR}$ IND GI CNIDC GI → BUFF MAR MODE MAR MODE NOOP MODE PAU RESET MASTER TESTS CMPT PS IRPT INH LOAD E-IND TEST M-NOOP TEST REQ I HSKLN T-LA HKL MODE RESET I HSCLN REQ LA HSKLN REQ RSET LA REQ	NO SPEC ACTION	ADV EN SEQ ADV EN E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND SET EXEC IDLES INTRPT NEXT INST T-IRPT INH LOAD I BOX HSCLN REQ T-LA HK MODE RESET I HK REQ LA HK REQ RST LA REQ
SCC	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVELAC 1-29-60 WCS

INDICATOR TRANSFER IC FOR STICA BIN

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	
TBC	57-033	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE	57-033 (W) NOOP MODE	ADV EN SEQ ADV EN SEQ LATE DEC EN LDE	DOES NOT APPEAR
ABC	57-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER E-IND TEST NORMAL M TEST MAR MODE RESET TBC AES DEC GO ALL IND & IC GI $\overline{XR}$ IND GI BUFF RESET SAU EN MEM	57-033 (W) NOOP MODE	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI BUFF E-IND TEST M-NOOP TEST MAR MODE NOOP MODE RESET SAU EN MEM RST PAU MASTER TESTS CMPT	DOES NOT APPEAR
SCC	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE	

I BOX PSEUDO STORE $\overline{TC}$

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	02-023	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC		DOES NOT APPEAR	PS EUDO STORE	ADV EN SEQ T-LA HSCLN IF IRPT ON IMM PREVIOUS INSTR, TBC WAITS FOR ABC TO RESET TC WHICH NEVER COMES
ABC	02-023	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI XR IND RESET-TBC AES		DOES NOT APPEAR		ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET LFL SET EXEC IDLES
SCC	XX-XX3	ADV EN SEQ RESET LFL				T-IRPT INH LOAD I BOX HSKLN REQ B T-LA HK MODE RST I HK REQ LA HK REQ RST LA REQ
		A+B SAMPLE REFERENCE				A+B SAMPLE REFERENCE

I BOX PSEUDO STORE IC

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT OPERATION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	02-033	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE DEC WAIT FOR ABC TO RESET FLP TC	02-133 02-133 NOOP MODE	ADV EN SEQ LATE DEC ENABLE INTERLOCK A-T	PSEUDO STORE	ADV EN SEQ T-LA HSCLN IF IRPT ON IMM PREVIOUS INSTR, TBC WAITS FOR ABC TO RESET TC WHICH NEVER COMES
ABC	02-033	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI XR IND GI XR IND GI → BUFF RESET PAU MASTER TESTS E-IND TEST M-NOOP TEST MAR MODE MAR MODE RESET TBC AES	02-133 02-033 NOOP MODE CMPT	ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI XR IND GI CNIDC GI → BUFF MAR MODE NOOP MODE RESET PAU MASTER TEST CMPT PS IRPT INH LOAD RESET LFL I-BOX HSKLN REQ B LA HK MODE RESET I HK REQ LA HK REQ E-IND TEST RST LA REQ M NOOP TEST SCC SEES 02-032 P.58		ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET LFL SET EXEC IDLES T-IRPT INH LOAD I BOX HSKLN REQ B TLA HK MODE RST I HK REQ LA HK REQ RST LA REQ
SCC	XX-XX3	ADV EN SEQ RESET LFL A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

I BOX INT FETCH IC

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSEHOLD ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	51-027	ADV EN SEQ ADV EN SEQ LATE DEC EN		DOES NOT APPEAR	EA BUSY LEV	ADV EN SEQ T-LA HSCLN MODE
ABC	51-027	ADV EN SEQ E-IND XFER M-IND DEC GO ALL IND & IC GI $\overline{XR}$ IND EE-A TIMER E-A TIMER M-A TIMER GO INT REG MAR MODE GI → LA RST EA BUSY CHK DATA OR $\overline{CHK}$ DATA RESET LFi		DOES NOT APPEAR	EA BUSY LEVEL	ADV EN SEQ AES E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND RESET EA BUSY SET NOOP i LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT+PS INT+BR REC) INH LOAD
SCC	51-026	ADV EN SEQ ADV EN SEQ ABC RESETS LFi LATE DEC EN E-LA I TIMER M-LA-I FOR NO INDEX XFER GO LAICIB→Y GI → Y RESET LFi GI LAPAR ERR TO I BOX COND MK IND FR LA PAR ERR A+B SAMPLE REFERENCE		DOES NOT APPEAR		A+B SAMPLE REFERENCE

LEVEL AC 1-29-60 WCS

I/O LEVEL $\overline{IC}$

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCK	LEVEL DESIGN	TIMING & INTERLOCKS	LEVEL DESIGN	TIMING & INTERLOCKS
TBC	20-003 (Bx) 24-003 (Hx)	ADV EN SEQ AES LATE DECODE EN. LDE DEC GO TOB EXCHG DEC GO OP CODE XCHG INTERLOCK TBC*ABC INTERLOCK ABC*SCC E-T TIMER M-T TIMER X ACCEPT OR REJECT X REACT STORAGE BUFFER SELECT BX/HSX I/O RESPONSE	20-103 24-103	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE INTERLOCK A-T	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN
ABC	20-003 (Bx) 24-003 (Hx)	ADV EN SEQ ADV E-IND XFER M IND XFER GI $\overline{XR}$ IND MAR MODE	20-103 24-103	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC IND MAR MODE T-NOOP MODE		ADV EN SEQ ADV EN E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND SET EXEC IDLES INTRPT NEXT INST T-IRPT INH LOAD I BOX HSCLN B REQ T-LA HK MODE RESET I HK REQ LA HK REQ RST LA REQ
SCC	APPEARS AS XX-XX3	ADV ENABLES SEQ RESET LF2 A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE	XX-XX3	A+B SAMPLE REFERENCE

I/O 2ND LEV $\overline{CCW}$ IC

COUNTER	NORMAL OPERATION		INSTR REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	25-033	ADV EN SEQ ADV LATE DEC EN LDE	25-033 Ⓦ NOOP MODE OR 25-133	ADV EN SEQ LDE LDE INTERLOCK A-T	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN MODE
ABC	25-033	ADV EN SEQ ADV EN SEQ E-XFER IND M-XFER IND DEC GO ALL IND & IC GI $\overline{XR}$ IND GI BUFF MAR MODE MAR MODE RESET PAU MASTER TESTS RESET TBC AES E-IND TEST M-NOOP TEST	25-133 OR 25-033 Ⓦ NOOP MODE CMPT	ADV EN SEQ ADV EN SEQ E-XFER IND M-XFER IND DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI BUFF MAR MODE MAR MODE RESET PAU MASTER TESTS & CMPT NOOP MODE E-IND TEST M-NOOP TEST		ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT & PS INT & BR REC) INH LOAD
SCC	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

I/O 2ND LEV CCW IC

COUNTER	NORMAL OPERATION		INSTR REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	65-033	ADV EN SEQ ADV LATE DEC EN LDE	65-133 OR 65-033 @ NOOP MODE	ADV EN SEQ LDE LDE INTERLOCK A-T	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN MODE
ABC	65-033	ADV EN SEQ ADV EN SEQ E-XFER IND M-XFER IND DEC GO ALL IND & IC GI $\overline{XR}$ IND GI BUFF MAR MODE MAR MODE RESET PAU MASTER TESTS CMPT RESET TBC AES E-IND TEST M-NOOP TEST	65-133 OR 65-033 @ NOOP MODE	ADV EN SEQ ADV EN SEQ E-XFER IND M-XFER IND DEC GO ALL IND & IC GI $\overline{XR}$ IND GI CNIDC GI BUFF MAR MODE MAR MODE RESET PAU MASTER TESTS CMPT NOOP MODE E-IND TEST M-NOOP TEST		ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND LA DISABLE IRPT LINE T-LA HSCLN MODE (IRPT&PS INT& BR REC) INH LOAD
SCC	XX-XX3	A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE		A+B SAMPLE REFERENCE

LEVEL AB 1-29-60 WCS

INTERRUPT TEST LEVEL $\overline{IC}$

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIGN	TIMING & INTERLOCKS	LEVEL DESIGN	TIMING & INTERLOCKS
TBC	00-023-1	ADV EN SEQ ADV EN SEQ LATE DEC EN LATE TBC WAIT FOR E·M OF IND XFER		WILL NOT APPEAR	NO SPEC ACTION	ADV EN SEQ T-LA HSCLN
ABC	00-023-1	ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC MAR MODE GI $\overline{XR}$ IND RST TBC/AES		WILL NOT APPEAR		ADV EN SEQ ADV EN E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC GI CNIDC IND SET EXEC IDLES INTRPT NEXT INST T-IRPT INH LOAD I BOX HSCLN^{B} REQ T-LA HK MODE RESET I HK REQ LA HK REQ RST LA REQ
SCC	XX-XX5	ADV EN SEQ RESET LF1 A+B SAMPLE REFERENCE			XX-XX3	A+B SAMPLE REFERENCE

INTERRUPT TEST LEVEL IC

COUNTER	NORMAL OPERATION		INSTRUCTION REJECT ACTION		HOUSECLEAN ACTION	
	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS	LEVEL DESIG	TIMING & INTERLOCKS
TBC	00-033-1	ADV EN SEQ ADV EN SEQ LATE DEC ENABLE		WILL NOT APPEAR	NO SPEC ACTION	ADV EN SEQ T-LA HK MODE
ABC		ADV EN SEQ ADV EN SEQ E-IND XFER M-IND XFER DEC GO ALL IND & IC MAR MODE MAR MODE GI $\overline{XR}$ IND E-IND TEST GI BUFF M-NOOP TEST RESET PAU MASTER TESTS CMPT RST TBC AES		WILL NOT APPEAR		ADV EN SEQ ADV EN SEQ E-HSCLN TIMER M-HSCLN TIMER DEC GO ALL IND & IC SET EX IDLES GI CNIDC INTRPT NEXT INST T-IRPT IN H LOAD I BOX HK REQ B T-LA HK MODE RST I HK REQ LA HK REQ RSET LA HK REQ
SCC	XX-XX3				XX-XX3	
		A+B SAMPLE REFERENCE				A+B SAMPLE REFERENCE

IRPT-BIN OP CODE LEVEL FOR IRPT BIT RESET

COUNTER	NORMAL OPERATION		INSTR REJ ACTION		RECOVERY ACTION	
	LEV DESIG		LEV DESIG			
TBC	75-023	SAME AS 01-003, PLUS DEC GO IRPT BIT TO EXEC REG	75-123	WILL NOT APPEAR		WILL NOT APPEAR
ABC	75-023	SAME AS 01-003, PLUS INHIBIT RESET T-LA DISABLE IRPT LINE	75-123	WILL NOT APPEAR		WILL NOT APPEAR
SEE	XX-XX3					

REAL EXT & IND STORE COUNTER OPERATION

COUNTER	LEVEL DESIG	NORMAL OPERATION TIMING & INTERLOCKS	
SCC EXT LAAR	17-032	ADV EN SEQ ADV EN SEQ	
	17-022	ABC RESET LATE DECODE ENABLE	
	23-032	LFi E-STORE CHK TIMER RESET LFi	
	23-022	M-ST CHK TIMER	
	21-032	GO LAICIB IF $\bar{O}\cdot\bar{4}$	
	13-032	GI TO LA	
	02-012	COND LA PAR ERR TO IND REG (IK)	
	21-022	CHK PAR IF $\bar{O}\cdot\bar{4}$	
		CHK IF O+4	
	33-032	T-ST CHK	
	33-022	SET FLP ST CHK TEST COMPLETE	
		LA STORE CHECK TEST	
		STO REQUEST ACCEPT	
		T-GO-LAMIB	
		E-DATA STORE TIMER	
		M-DATA	
		RESET EA BUSY STORE TIMER	
		STORE EXECUTED	
SCC IND LAAR	17-032	ADV EN SEQ ADV	
	17-022	ABC RESET LATE DEC EN	
	23-032	LFi E-LA-I TIMER RESET LFi	
	23-022	M-TIMER FOR INDEX XFER	
	21-032	GO LAAR TO I BOX	
	13-032	GO LAICIB	
	02-012	GI → X	
	21-022	COND LA PAR ERR TO IND REG (IK)	
		CHK PAR	
		T-ST CHK	
		SET FLP ST CHK TEST COMP	
		M-ST CHK TEST	
		CLEAR INDEX E A	
		B B CL INDEX M	
		WRITE INDEX E A A	
		B WR. INDEX M	
		RST EABZY	
		STO EXEC'D	
		INDEX STORE REG TO YCS	
		A+B SAMPLE REFERENCE	

VFL IB OR BB SCC BR RECOVERY

COUNTER	LEVEL DESG	NORMAL OPERATION TIMING & INTERLOCKS	
SCC	45-032 T-LA HSCLN	ADV EN SEQ ADV EN SEQ LATE DEC EN E-LA-I TIMER M-LA-I TIMER FOR NO INDEX XFER GO LAICIB GI-Y RESET LFL CND MK FR LA PAR ERR	
		A+B SAMPLE REFERENCE	

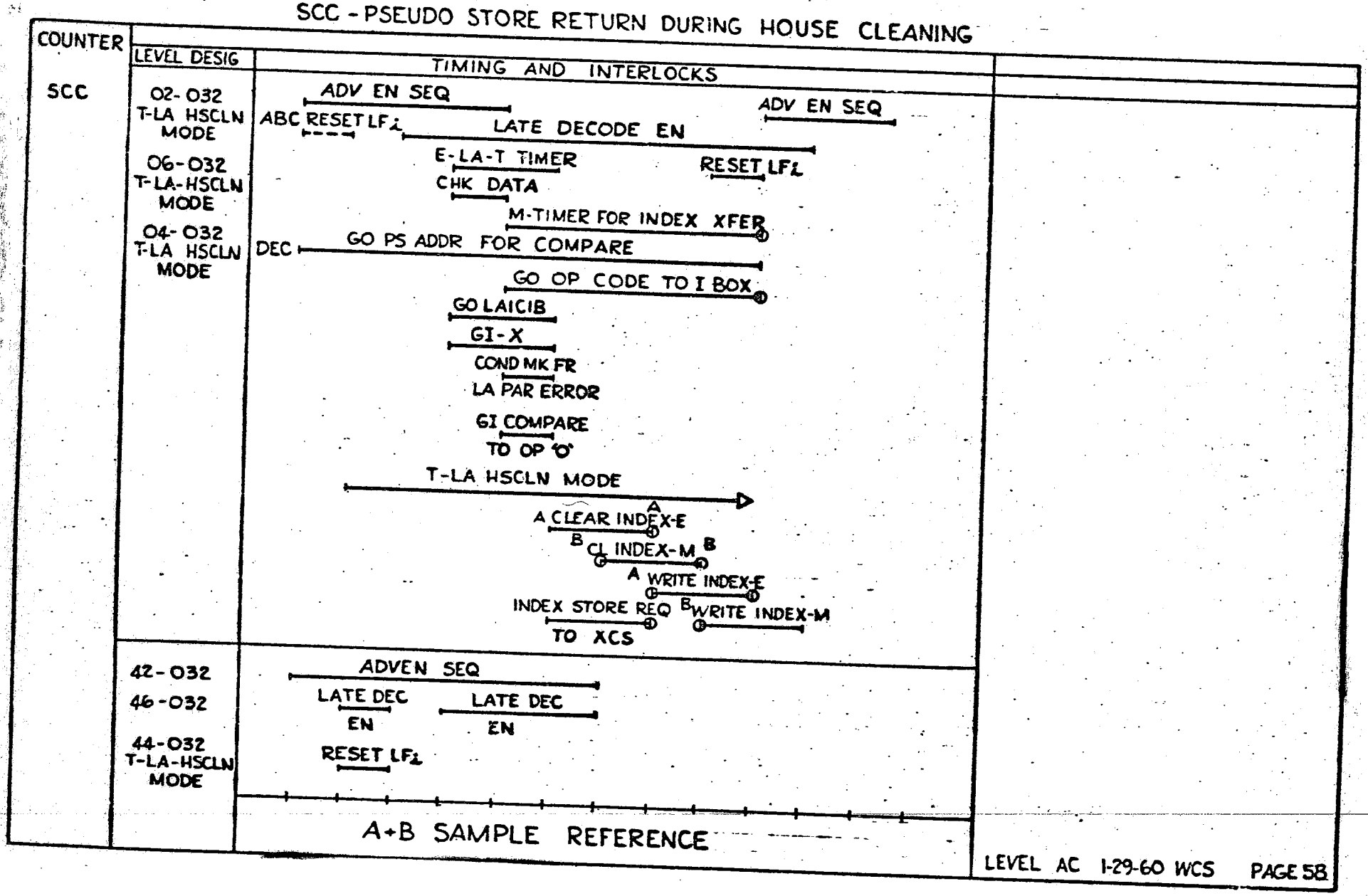
I BOX STORE EXT

COUNTER	LEVEL DESIG	NORMAL OPERATION TIMING & INTERLOCKS
SCC	33-072	ADV EN SEQ ADV EN SEQ ABC SETS LF LATE DEC EN ST REQ
	33-062	ST ACCEPT
	31-072	T-GO LAMIB E-ST DATA TIMER M-ST DATA T-STORE EXECUTED RESET EA BUSY RESET LF

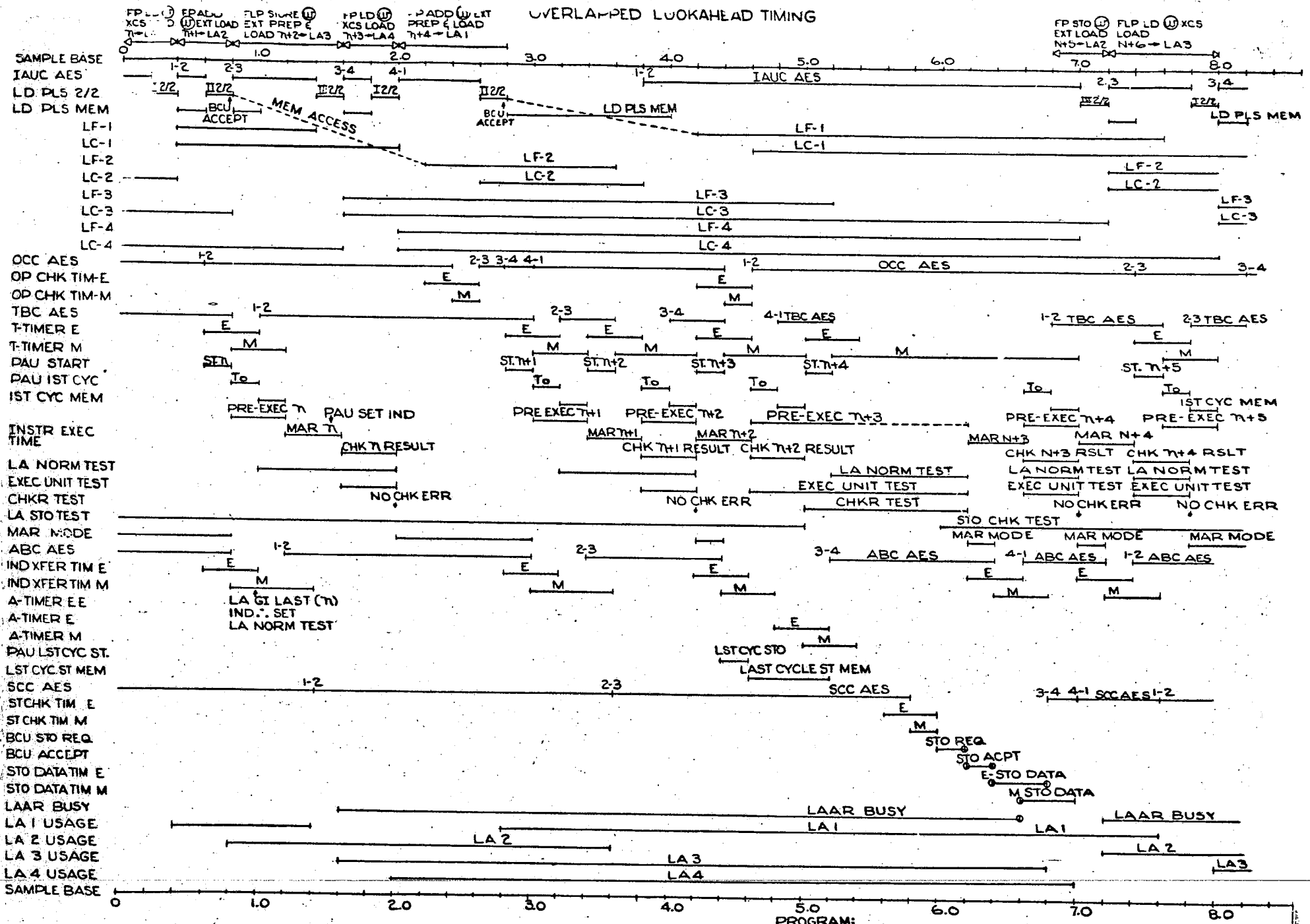
A+B SAMPLE REFERENCE

LEVEL AB 10-27-59 WCS

SCC - PSEUDO STORE RETURN DURING HOUSE CLEANING



OVERLAPPED LOOKAHEAD TIMING



LEVEL A-B W.C.S.
1/29/60